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DEFENSE SYSTEMS MANAGEMENT SCHOOL

PROGRAM MANAGEMENT COURSE

INDIVIDUAL STUDY PROGRAM

(6) MICROPROCESSOR TECHNOLOGY FOR MANAGERS

(9) STUDY PROJECT REPORT PMC 76-1

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(11) May 76

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DEFENSE SYSTEMS MANAGEMENT SCHOOL

STUDY TITLE:

MICROPROCESSOR TECHNOLOGY FOR MANAGERS

STUDY PROJECT GOALS:

TO EXPLORE IN NARRATIVE FORM MICROPROCESSOR TECHNOLOGY, TO INCLUDE ARCHITECTURE, ORGANIZATION, MEMORIES AND THE GENERAL CAPABILITIES AND LIMITATIONS IN THIS NEW FIELD.

TO PROVIDE MANAGEMENT PERSONNEL WITH A CURRENT GUIDE TO MICRO-PROCESSOR REFERENCES.

STUDY REPORT ABSTRACT:

THIS REPORT REPRESENTS THE EFFORTS OF THE AUTHOR TO GAIN A BETTER UNDERSTANDING OF MICROPROCESSOR TECHNOLOGY IN EARLY 1976. THIS FIELD IS ONLY SIX YEARS OLD AND IS DEVELOPING RAPIDLY. BY 1980 THE MICROPROCESSOR/MICROCOMPUTER INDUSTRY WILL REPRESENT APPROXI-MATELY $1 BILLION ANNUALLY. A LITERATURE SURVEY AND INTERVIEWS WITH MANUFACTURERS AND APPLICATION ENGINEERS PROVIDED A TIMELY UPDATE ON THIS TECHNOLOGY.

THE NARRATIVE DISCUSSES MICROPROCESSOR STRUCTURE AND ORGANIZATION, INTERFACING, CAPABILITIES, LIMITATIONS, AND TYPICAL APPLICATIONS. SINCE THERE ARE MANY MICROPROCESSORS, THE MOTOROLA 6800 WAS CHOSEN AS A REPRESENTATIVE SYSTEM. THE 6800 DOES NOT REPRESENT A LARGE SHARE OF THE MARKET CURRENTLY BUT APPEARS TO BE ONE OF THE MOST LIKELY MICROPROCESSORS TO BE USED IN THE NEXT FEW YEARS.

IN ADDITION TO THE NARRATIVE DISCUSSION OF MICROPROCESSOR TECH-NOLOGY, A GLOSSARY OF MICROPROCESSOR TERMINOLOGY, A COMPREHEN-SIVE LIST OF MICROPROCESSOR COMPANIES AND AN ANNOTATED BIBLIO-GRAPHY BY YEAR ARE APPENDED.

THIS REPORT PROVIDES THE MANAGER WITH A BRIEF UPDATE ON MICRO-PROCESSOR TECHNOLOGY IN THE 1976 TIME FRAME. THIS INFORMATION SHOULD BE UPDATED PERIODICALLY TO BE OF MAXIMUM VALUE.

KEY WORDS: MICROPROCESSOR, MICROCOMPUTER

DATA PROCESSING

MATERIEL DESIGN AND DEVELOPMENT COMPUTERS
SYSTEMS MANAGEMENT MINICOMPUTERS

NAME, RANK, SERVICE	CLASS	DATE
STUART G. MITCHELL, LTC, USA	PMC 76-1	MAY 1976

EXECUTIVE SUMMARY

THE AGE OF VACUUM TUBES WAS REPLACED BY THE AGE OF TRANSISTORS IN THE THIRD QUARTER OF THIS CENTURY. THE FOURTH QUARTER WILL BE KNOWN AS THE AGE OF MICROPROCESSORS. WHAT IS A MICROPROCESSOR? A MICROPROCESSOR/MICROCOMPUTER CAN BE THOUGHT OF AS A SMALL COMPUTER. IT DIFFERS FROM A DESK CALCULATOR IN THAT IT HAS: A RANDOM ACCESS MEMORY; A CONTROLLABLE INPUT/OUTPUT SYSTEM; A REPERTORY OF INSTRUCTION TO ALLOW; MANIPULATION OF WORDS STORED IN MEMORY; MODIFICATION OF ANY BIT IN A WORD; TRANSFERRING THE CONTROLS OF A PROGRAM BY BRANCHING; AND CONTROLLING EXTERNAL EQUIPMENT WITH THE AID OF AN INTERRUPTION FACILITY. THE 1976 COST OF A TYPICAL MICROPROCESSOR INTEGRATED CIRCUIT IS $25. A TYPICAL MICROCOMPUTER SYSTEM WOULD BE IN THE ORDER OF $500.

FROM AN ARCHITECTURAL STANDPOINT, MICROPROCESSORS ARE DIVIDED INTO: SINGLE-CHIP CONTROLLERS, 4-BIT, 8-BIT, 16-BIT, AND BIT-SLICE CONFIGURATIONS. THE MOST COMMON BEING THE 8-BIT FAMILY AND BIT-SLICE TYPES BEING USED TO BUILD MACHINES OF VARYING BIT LENGTHS.

SINCE MICROPROCESSORS CURRENTLY DO NOT CONTAIN THEIR OWN MEMORY, SEMICONDUCTOR MEMORIES ARE IMPORTANT TO A DISCUSSION OF MICROPROCESSORS. SEMICONDUCTOR MEMORIES ARE DIVIDED INTO THREE CATEGORIES: RANDOM ACCESS; READ ONLY; AND SERIAL. RANDOM ACCESS MEMORIES ARE OF TWO TYPES: STATIC AND DYNAMIC. READ ONLY MEMORIES CAN BE MADE ELECTRICALLY PROGRAMMABLE OR

PERMANENTLY PROGRAMMED. SERIAL MEMORIES ARE MOSTLY OF THE SHIFT REGISTER TYPE. THE STATE OF THE ART IS BETWEEN 4K AND 16K BITS PER INTEGRATED CIRCUIT CHIP.

MICROPROCESSOR SELECTION VERSUS SELECTION OF A LARGER COMPUTER SHOULD BE BASED ON INPUT/OUTPUT PARAMETER, PROCESSING SPEED, AND SPECIAL CONSTRAINTS SUCH AS SIZE, TEMPERATURE AND COST.

MICROPROCESSORS ARE BEING USED IN FOUR APPLICATIONS AREAS: DATA ACQUISITION AND CONTROL; DATA COMMUNICATION; HUMAN INTERFACE EQUIPMENT (TERMINALS, POINT-OF-SALE, ETC.); AND COMPUTATION. EACH OF THESE AREAS STRESSES CERTAIN MICROPROCESSOR CHARACTERISTICS SUCH AS WORD LENGTH, NUMBER CRUNCHING ABILITY, SPEED, ABILITY TO REACT IN REAL TIME, INTERRUPT CAPABILITY, LOW COST, HIGH RELIABILITY, BCD ARITHMETIC ABILITIES, USER PROGRAMMABILITY, AND EASE OF INTERFACING TO ANALOG SIGNAL SOURCES.

ADVANCED CHEMISTRY ANALYZERS, ELECTRONIC CONTROL SYSTEM FOR BARS, TALKING CALCULATORS FOR THE BLIND, ROBOT INDUSTRIAL TOOLS, AUTOMATIC SCORERS FOR USE IN BOWLING ALLEYS ARE PRACTICAL EXAMPLES OF EXISTING MICROPROCESSOR APPLICATIONS. FUTURE APPLICATIONS APPEAR TO BE BOUNDLESS; HOWEVER, CURRET EFFORT APPEARS TO BE IN THE APPLICATION OF MICROPROCESSORS TO THE HOME APPLIANCE/CONTROL AREA. EXAMPLES BEING COOKING RANGES, WASHING MACHINES, AND AUTOMATIC UTILITY METER READERS. THE 1980 PROJECTED MARKET FOR MICROPROCESSORS IS $450. MILLION.

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MICROPROCESSOR TECHNOLOGY FOR MANAGERS

GETTING A GOOD GRIP ON THE SUBJECT OF MICROPROCESSORS IS THE BIGGEST AND MOST EXCITING CHALLENGE FACING AN ELECTRONICS MANAGER TODAY. FOR ALL ITS FASCINATION AND ALLURE, THE SUBJECT IS SO COMPLEX AND ITS IMPACT SO FAR REACHING THAT A LOT OF ENERGY IS NEEDED TO ENCOMPASS IT ALL. COUNPOUNDING THE PROBLEM IS THE DYNAMIC NATURE OF MICROPROCESSOR DEVELOPMENTS. NEW COMPONENTS, NEW TECHNIQUES, NEW APPLICATIONS AND NEW MARKETS ARE APPEARING AT A STEADILY ACCELERATING PACE. {46, 37, 17, 15} A MICROPROCESSOR IS A TOOL WHOSE VERSATILITY AND POWER EXCEED ANYTHING ELECTRONIC ENGINEERS HAVE EVER HAD AT THEIR DISPOSAL. FOR THOSE WHO ARE JUST GETTING ON BOARD, THIS REPORT WILL BE A HELPFUL GUIDE TO THE REALITIES OF MICROPROCESSORS. IT IS THE INTENT OF THE REPORT TO FAMILIARIZE THE READER WITH MICROPROCESSOR HIERARCHY, STRUCTURE AND ORGANIZATION, INTERFACING CAPABILITIES, LIMITATIONS AND APPLICATIONS. APPENDIX A IS A GLOSSARY OF MICROPROCESSOR TERMS. {61}*

IN EVERDAY TERMS, THE MEANING OF MICROPROCESSOR TECHNOLOGY IS THREEFOLD: 1. CHEAP DIGITAL COMPUTING CAPABILITY CAN BE PUT ANYWHERE; 2. FOR ANY DIGITAL SYSTEM, MICROPROCESSORS CAN GREATLY REDUCE THE COMPONENT COUNT; 3. ENGINEERING TURNAROUND TIME IS CUT DRASTICALLY. THESE SIMPLE TRUTHS ACCOUNT FOR THE CURRENT EXPLOSION IN MICROPROCESSOR ACTIVITY. PRACTICALLY ALL

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* {61} ALL REFERENCES ARE IN THE LIST OF REFERENCES SECTION ALPHABETICALLY BY YEAR. THE NUMBER IN { } IS THE SAME AS THE NUMBER IN THE REFERENCE SECTION.

NEW DATA PROCESSING SYSTEMS AT OR BELOW WHAT ONE COULD CALL THE MINICOMPUTER LEVEL OF COMPLEXITY ARE BEING DESIGNED WITH MICROPROCESSORS. IT HAS BEEN ESTIMATED THAT BY 1980 MICROPROCESSOR-BASED-SYSTEMS AND EQUIPMENT WILL EXCEED $1 BILLION IN SALES. {07, 58}

MICROPROCESSOR HIERARCHY

LESS THAN THIRTY YEARS AGO, ELECTRICAL ENGINEER J. PRESPER ECKERT, JR. AND PHYSICIST JOHN W. MAUCHLY, AT TIMES ASSISTED BY AS MANY AS FIFTY HELPERS, LABORIOUSLY BUILT THE WORLD'S FIRST ELECTRONIC DIGITAL COMPUTER. THEIR ELECTRONIC NUMERICAL INTEGRATER AND COMPUTER {ENIAC} WAS A FICKLE MONSTER THAT WEIGHED THIRTY TONS AND RAN ON EIGHTEEN THOUSAND VACUUM TUBES - WHEN IT RAN. BUT IT STARTED THE COMPUTER REVOLUTION.

THE THIRD QUARTER OF THE TWENTIETH CENTURY WAS MARKED BY MANY MILESTONES. AMONG THE MOST SIGNIFICANT WERE THE INVENTION AND SUBSEQUENT PERVASIVENESS OF THE TRANSISTOR AND ITS INEVITABLE PROGENY, THE INTEGRATED CIRCUIT. IT BECAME KNOWN, AMONG OTHER THINGS, AS THE AGE OF THE TRANSISTOR. WHETHER OR NOT THE DEVELOPMENT OF THE MICROPROCESSOR, AND THE MICROCOMPUTER IT SPAWNS, IS ULTIMATELY JUDGED AS GREAT A BREAKTHROUGH AS THE UBIQUITOUS TRANSISTOR IS OF LITTLE CONSEQUENCE. THERE IS LITTLE OR NO DOUBT THAT ITS INFLUENCE WILL BE HUGE. THE CHANGES IT CREATES WILL BE PERSONAL AND PROFESSIONAL, PUBLIC AND PRIVATE, INDIVIDUAL AND INSTITUTIONAL, GREAT AND SMALL. THEY WILL BE

SUCH THAT THE FINAL QUARTER OF THIS CENTURY SURELY WILL BE KNOWN, IN ITS TURN, AS THE "AGE OF THE MICROPROCESSOR."(06, 08, 21, 27)

THERE ARE THREE TYPES OF COMPUTERS: ANALOG, DIGITAL AND HYBRID. MICROPROCESSORS ARE OF THE DIGITAL TYPE AND ARE CAPABLE OF STORING AND PROCESSING INFORMATION IN DIGITAL FORM. THIS DEFINITION IS NOT SUFFICIENT BECAUSE IT WOULD IMPLY THAT A DESK CALCULATOR WAS A MEMBER OF THE COMPUTER FAMILY. THIS IS INCORRECT BECAUSE THERE IS AN ESSENTIAL DIFFERENCE BETWEEN A COMPUTER AND THE CALCULATOR: THE FIRST IS CAPABLE OF CARRYING OUT ANY OPERATION WHEREAS THE SECOND CAN ONLY PERFORM THE FUNCTION THAT WAS PERMANENTLY ASSIGNED TO IT WHEN IT WAS BUILT. THE ABILITY OF THE COMPUTER TO ACCOMPLISH A VARIETY OF TASKS DICTATED BY A SERIES OF INSTRUCTIONS HAS A COUNTER PART: THE NEED TO PROGRAM IT AND THEREFORE TO KNOW THE LANGUAGE WHICH THE COMPUTER CAN ACCEPT. THIS DISTINCTION BETWEEN THE COMPUTER AND THE CALCULATOR ALLOWS US TO MAKE A BETTER DEFINITION. A HARDWARE SYSTEM WILL BE DESIGNATED "COMPUTER" WHEN: 1. IT HAS A RANDOM ACCESS MEMORY FOR READ/WRITE OPERATIONS; 2. IT HAS A CONTROLLABLE INPUT/OUTPUT SYSTEM; 3. ITS REPERTORY OF INSTRUCTIONS ALLOW: (A) THE MANIPULATION OF WORDS STORED IN MEMORY, (B) THE MODIFICATION OF ANY BIT IN A WORD, (C) TRANSFERRING THE CONTROLS OF A PROGRAM BY BRANCHING, (D) CONTROLLING EXTERNAL EQUIPMENT WITH THE AID OF AN INTERRUPTION FACILITY. (12, 24)

COMPUTERS - MINICOMPUTERS - MICROCOMPUTERS - MICROPROCESSORS

APPEARS TO BE THE NORMAL HIERARCHY. THE DIVIDING LINE BETWEEN THESE RELATED MACHINES IS NORMALLY EXPRESSED IN SIZE, DOLLARS OR BOTH. FOR THE PURPOSE OF THIS REPORT, A MICROCOMPUTER WILL, BY DEFINITION, CONTAIN AT LEAST ONE MICROPROCESSOR. DEC'S ANDREW C. KNOWLES HAS QUIPPED THAT, "MINICOMPUTER VENDORS MAKE MINICOMPUTERS AND SEMICONDUCTOR VENDORS MAKE MICROCOMPUTERS." {10, 44} IN 1975 A MINICOMPUTER INCLUDED A CPU WITH AT LEAST 4K WORDS OF MEMORY AND COST $1600 OR MORE AND HAD A SPEED LIMITED BY THE SPEED OF THE MEMORY. A MICROCOMPUTER CONSISTED OF A CPU OF 1K WORDS OF MEMORY, COST LESS THAN $1000 AND HAD A SPEED LIMITED BY THE PROCESSOR. CURRENTLY THE COST DIFFERENTIAL HAS BEEN REDUCED TO $500. IF ONE IS TO CONSIDER ONLY THE MICROPROCESSOR/CPU CHIP, THE COSTS ARE CURRENTLY RUNNING BETWEEN $15 AND $69. PROJECTIONS FOR 1979 INDICATE THAT COST OF THE MICROPROCESSOR CHIP WILL BE BETWEEN $2 AND $10. THIS REDUCTION IN COST IS ATTRIBUTABLE TO INCREASED SALES VOLUME AND PARALLELS THE COST REDUCTION IN THE SEMICONDUCTOR MARKET. AT THE PRESENT TIME, THE COST OF A TYPICAL MICROCOMPUTER SYSTEM, WHICH IS IN THE ORDER OF $500, CONSISTS MAINLY OF SUPPORT EQUIPMENT COSTS, I.E., POWER SUPPLIES, MEMORY, INTERFACE DEVICES, CABINETS, ETC. FUTURE PROJECTIONS FOR MICROCOMPUTER SYSTEMS DO NOT INDICATE SUBSTANTIAL REDUCTION IN COST SINCE THE PRICES FOR SUPPORT EQUIPMENT HAVE ALREADY BOTTOMED OUT. IT SHOULD BE NOTED THAT THE COST OF THE MICROPROCESSOR IS ALREADY LESS THAN 5% OF THE SYSTEM COST. {44, 45}

STRUCTURE AND ORGANIZATION

THE STRUCTURE AND ORGANIZATION OF MICROPROCESSORS IS STILL IN AN EVOLUTIONARY PHASE SINCE THE FIRST MICROPROCESSOR IS ONLY SEVEN YEARS OLD. THE ARCHITECTURE AND PERFORMANCE OF TODAY'S MICROPROCESSORS IS AIMED AT SPECIFIC APPLICATIONS. THE SMALLEST SYSTEMS ARE DESIGNED TO REPLACE ELECTRO-MECHANICAL CONTROLLERS. THE LARGER MICROPROCESSOR SYSTEMS ARE AIMED AT MINICOMPUTER APPLICATIONS. {22} FROM AN ARCHITECTURAL STANDPOINT, TODAY'S MICROPROCESSORS ARE DIVIDED INTO FIVE MAJOR DIVISIONS: 1. THE SINGLE CHIP CONTROLLER {NOT UNLIKE A CALCULATOR}; 2. THE FOUR-BIT FAMILY; 3. THE EIGHT-BIT FAMILY; 4. THE SIXTEEN-BIT FAMILY; 5. THE BIT-SLICE FAMILY. THE FIRST FOUR ARE READILY APPARENT, HOWEVER, THE FIFTH MAY NEED SOME EXPLANATION. THE BIT-SLICE FAMILY ARCHITECTURE CONSISTS OF A MICROPROCESSOR CHIP WHICH CONTAINS AND PROCESSES TYPICALLY FOUR BITS AT A TIME. THESE SLICES MAY BE PARALLELLED TO PRODUCE A MACHINE OF ANY SIZE; FOR EXAMPLE, EIGHT FOUR-BIT SLICES WOULD YIELD A THIRTY-TWO-BIT MICROPROCESSOR. THE UNIVERSE OF MICROPROCESSORS CURRENTLY ON THE MARKET IS SHOWN IN FIGURE 1. {41,54,55}

AS CAN BE SEEN FROM FIGURE 1, THE EIGHT-BIT FAMILY IS BY FAR THE MOST POPULAR. {32} THE MICROPROCESSORS MANUFACTURED BY INTEL, MOTOROLA AND TEXAS INSTRUMENT OCCUPY 95% OF THE CURRENT MARKET. {03, 04} APPENDIX B CONTAINS A LIST OF ALL KNOWN MICROPROCESSOR MANUFACTURERS. {11}

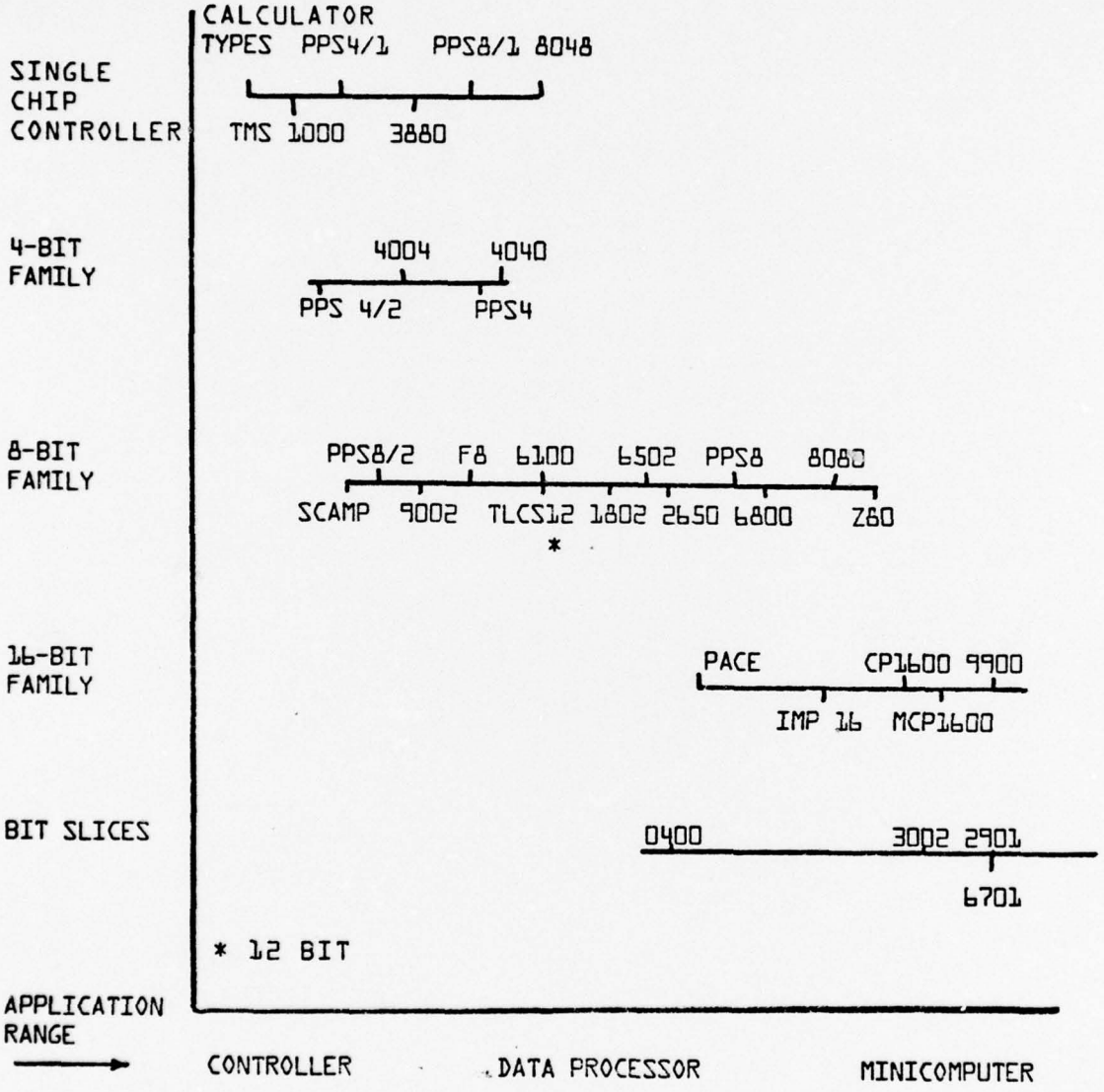

FIGURE 1. THE MICROPROCESSOR UNIVERSE APRIL 1976

THE INTERNAL ARCHITECTURE OF THE VARIOUS MICROPROCESSORS IS CONSIDERABLY DIFFERENT AS ARE THE EXTERNAL INTERFACES; HOWEVER, THEY CAN BE MADE FUNCTIONALLY COMPATIBLE AT THE SYSTEMS LEVEL. THE FIRST MICROPROCESSOR ARCHITECTURE TO WIN ACCEPTANCE WAS INTEL'S 8008. THE 8008 WAS REPLACED BY THE 8080 WHICH OCCUPIES 50% OF THE 1976 MICROPROCESSOR MARKET. THE NEXT MOST POPULAR ARCHITECTURE IS THE MOTOROLA 6800. THE 6800 OCCUPIES APPROXIMATELY 15% OF THE 1976 MARKET AND WILL BE USED AS A REPRESENTATIVE MICROPROCESSOR FOR DISCUSSION PURPOSES IN THIS PAPER. [09]

FIGURE 2 INDICATES THE INTERNAL ORGANIZATION OF THE MOTOROLA 6800 MICROPROCESSOR. AS WITH ANY MICROPROCESSOR, THE IMPORTANT AREAS OF CONSIDERATION ARE: 1. THE NUMBER OF REGISTERS, 2. THE NUMBER AND TYPES OF COUNTERS, 3. THE INSTRUCTION WORD SIZE, 4. THE DIRECT ADDRESSING CAPABILITY, 5, THE CLOCKING CAPABILITY, 6. THE INTERRUPT CAPABILITY AND 7. THE TOTAL ADD TIME. GIVEN THESE PERFORMANCE CHARACTERISTICS, ONE CAN MAKE A PRELIMINARY ASSESSMENT OF THE MICROPROCESSOR'S SUITABILITY. THE MOTOROLA 6800 ARCHITECTURE HAS BEEN CHOSEN FOR ITS SIMPLICITY BY MANY COMPANIES. [01] IT IS PREDICTED THAT BY 1979 IT WILL OCCUPY 40% OF THE MICROPROCESSOR MARKET. IT IS VERY INTERESTING TO NOTE THAT MANY MICROPROCESSORS ARE NOW BEING SECOND-SOURCED. THE 6800 CURRENTLY IS MANUFACTURED BY MOTOROLA, AMI AND HITACHI; AND, THERE ARE SEVERAL OTHER 6800 BASED SYSTEMS, NAMELY THE 6500 FAMILY BY MOS TECHNOLOGY AND SYNERTEK.

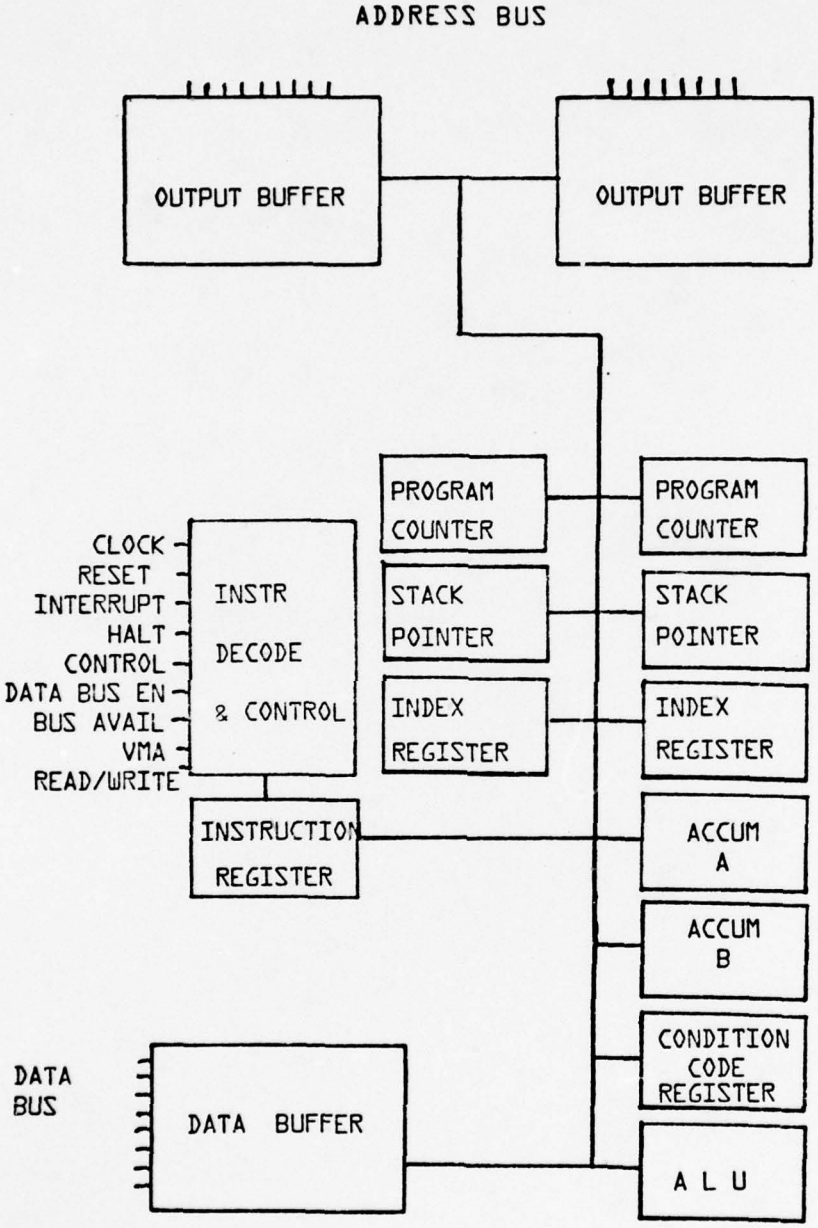

FIGURE 2. INTERNAL ORGANIZATION OF THE MOTOROLA 6800

RETURNING TO THE PERFORMANCE CHARACTERISTICS, DATA WORD SIZE (BITS) INDICATES THE LIMITS OF INFORMATION UNITS THAT CAN BE CONVENIENTLY PROCESSED, SINCE FEW CURRENT MICROPROCESSORS CAN OPERATE UPON MULTIPLE WORDS WITHOUT EMPLOYING MULTIPLE INSTRUCTIONS.

INSTRUCTION WORD SIZE IS AN INDICATION OF THE NUMBER OF BITS REQUIRED TO CONSTRUCT AN EXECUTABLE INSTRUCTION. IT IS NEARLY ALWAYS SOME MULTIPLE OF THE DATA WORD SIZE. USUALLY ONE-WORD INSTRUCTIONS REQUIRE LESS EXECUTION TIME THAN TWO-WORD INSTRUCTIONS WHICH IN TURN TAKE LESS TIME THAN THREE-WORD INSTRUCTIONS. BUT, THE LONGER THE INSTRUCTION, THE MORE COMPLEX THE OPERATION ITS EXECUTION CAN ACCOMPLISH.

ADD TIME (REGISTER TO REGISTER) IS THE MINIMUM TIME, IN MICRO SECONDS, THAT IT TAKES TO ADD TWO OPERANDS ALREADY PRESENT IN REGISTERS, LEAVING THE SUM IN ONE REGISTER. DO NOT FORGET THAT IT TAKES TIME TO PLACE THE OPERAND IN THE REGISTER.

THE NUMBER OF REGISTERS IS AN IMPORTANT CATEGORY BECAUSE THEY DETERMINE THE EASE WITH WHICH COMPUTATION MAY TAKE PLACE. DEPENDING UPON THE APPLICATION, ONE SHOULD INVESTIGATE ARITHMETIC REGISTERS, INDEX REGISTERS, GENERAL PURPOSE REGISTERS, AS WELL AS STACKED REGISTERS.

THE NUMBER OF DIRECTLY ADDRESSABLE INSTRUCTION WORDS INDICATES THE MAXIMUM SIZE OF A TASK WHERE INDIRECT ADDRESSING IS NOT USED. DIRECT ADDRESSING IS ACCESSING MEMORY WITH AN ADDRESS THAT IS EITHER EXPLICIT IN AN INSTRUCTION OR ARRIVED AT

THROUGH AUTOMATIC COMBINATION OF A REGISTER'S CONTENTS AND A PORTION OF AN INSTRUCTION. THE LATTER IS KNOWN AS INDEXING. THIS IS IN CONTRAST TO INDIRECT ADDRESSING, IN WHICH THE COMPUTER IS DIRECTED TO A MEMORY LOCATION WHEREIN LIES THE ADDRESS THAT WILL BE USED TO LOCATE AN OPERAND.

CLOCK FREQUENCY (HERTZ) IS THE NUMBER OF CLOCK CYCLES PER SECOND OF THE FUNDAMENTAL DRIVING CIRCUIT. DO NOT CONFUSE THIS CLOCK WITH A REAL-TIME CLOCK. THE NUMBER OF PHASES PER CYCLE TELLS YOU HOW MANY CLOCK PERIODS ARE REQUIRED TO COMPLETE ONE BASIC CPU OPERATION. FOR EXAMPLE, A MICROPROCESSOR USING A FIVE MEGAHERTZ CLOCK WOULD HAVE A CLOCK PERIOD OF 200 NANOSECONDS; IF THE CPU USED FOUR PHASES PER CYCLE, THEN 800 NANOSECONDS WOULD BE REQUIRED FOR A BASIC CPU OPERATION.

INTERRUPT CAPABILITY INDICATES HOW THE CPU RESPONDS TO THE ENVIRONMENT. IF THE CPU CANNOT BE INTERRUPTED, IT CANNOT BE USED EFFECTIVELY IN A REAL-TIME ENVIRONMENT.

DIRECT MEMORY ACCESS IS THE CAPABILITY OF THE PROCESSOR TO ALLOW INPUT/OUTPUT TO PROCEED CONCURRENTLY WITH, AND INDEPENDENTLY FROM, ITS OWN PROCESSING OPERATION. WITHOUT DIRECT MEMORY ACCESS, A PROCESSOR MUST PERFORM A NONCONCURRENT SUBROUTINE FOR EACH CHARACTER OF I/O DATA TRANSFERRED IN OR OUT. THIS PROCESS IS CALLED PROGRAMMED I/O.

USING THESE CRITERIA, THE MOTOROLA 6800 WOULD BE DESCRIBED AS HAVING EIGHT-BIT DATA WORD SIZE; EIGHT, SIXTEEN OR TWENTY-FOUR-BIT INSTRUCTION SIZE; TWO-PHASE, ONE MEGAHERTZ CLOCK;

TWO MICRO SECOND ADD TIME; TWO EIGHT-BIT ARITHMETIC REGISTERS; ONE SIXTEEN-BIT INDEX REGISTER; TWO EIGHT-BIT GENERAL PURPOSE REGISTERS; AND 65K WORDS OF DIRCTLY ADDRESSABLE MEMORY. SEE FIGURE 2.

REFERENCE [48] PROVIDES THE SPECIFICATIONS IN TABULAR FORM FOR THE CURRENT MICROPROCESSORS. THIS LIST IS UPDATED ANNUALLY AND CAN BE FOUND IN MOST TECHNICAL LIBRARIES.

SINCE THE MICROPROCESSOR/CPU IS OF LITTLE VALUE WITHOUT MEMORY, WE WILL LOOK AT THE VARIOUS TYPES OF MEMORY DEVICES NEXT.

MICROPROCESSOR MEMORIES

DEVELOPMENTS IN THE SEMICONDUCTOR INDUSTRY DURING THE LAST SIX YEARS HAVE CAUSED MAJOR SHIFTS IN THE TYPE OF STORAGE TECHNOLOGY USED IN DIGITAL SYSTEMS. SEMICONDUCTOR MEMORIES USED TODAY ARE LOWER IN COST, HIGHER IN DENSITY, FASTER IN ACCESS AND CYCLE TIME, HIGHER IN RELIABILITY AND MORE MODULAR IN INCREMENTAL SIZE THAN THE COMPARIBLE CORE MEMORY MODULES THAT ARE AVAILABLE. THE ADVANTAGES OF SEMICONDUCTOR MEMORIES HAVE BEEN SO WIDELY ACCEPTED THAT SEMICONDUCTOR MEMORY SHIPMENTS EXCEEDED CORE MEMORY SHIPMENTS IN LATE 1975. FIGURE 3 SHOWS THE CHANGE IN THE MEMORY MARKET AND THE INCREASING IMPORTANCE OF SEMICONDUCTOR MEMORY. THIS SHIFT IS THE RESULT OF MICROPROCESSOR BASED SYSTEMS. [43, 48, 56]

SEMICONDUCTOR MEMORIES ARE DIVIDED INTO THE THREE BROAD

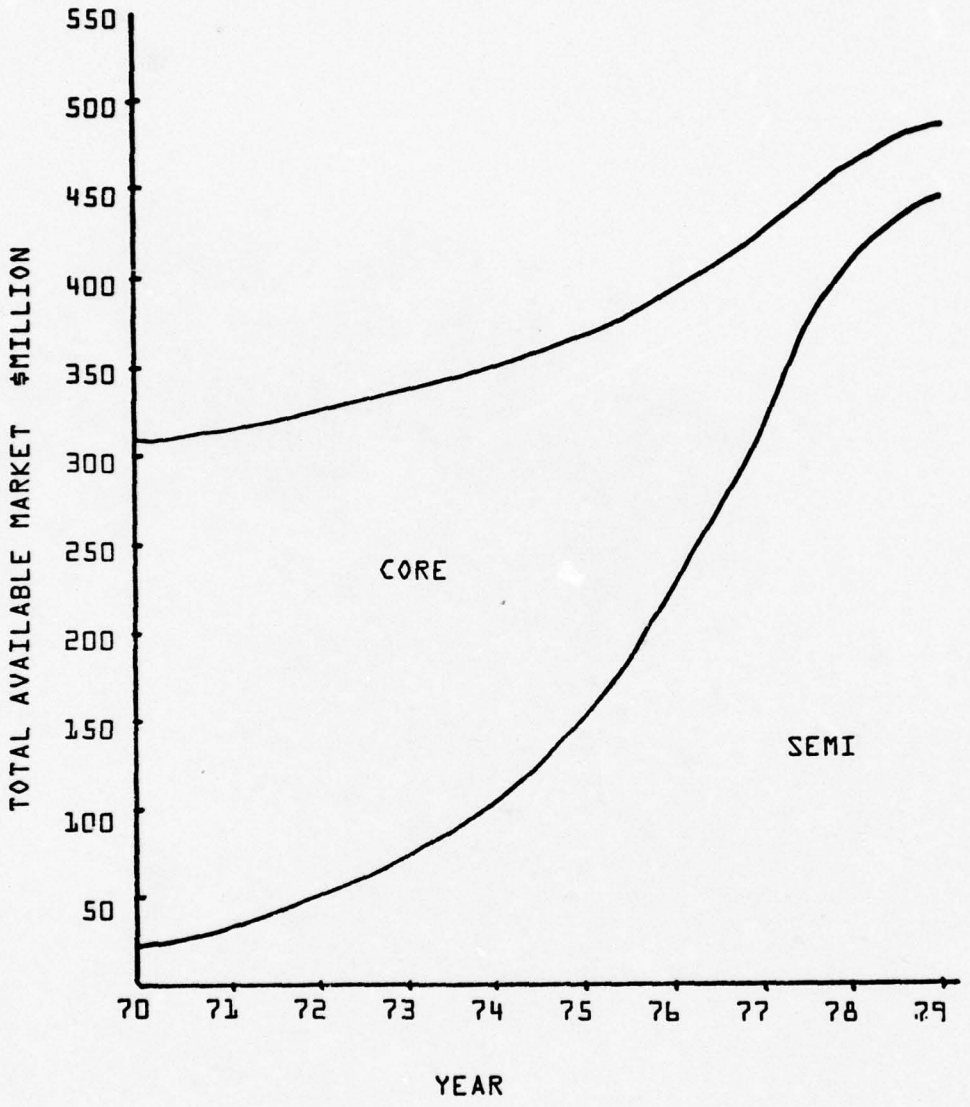

FIGURE 3. TOTAL AVAILABLE MEMORY MARKET [03]

CATEGORIES DEPICTED IN FIGURE 4. WITH TWO EXCEPTIONS, EACH OF THESE GENERIC CATEGORIES CAN BE IMPLEMENTED UTILIZING EITHER OF THE TWO MAJOR SEMICONDUCTOR TECHNOLOGIES: MOS OR BIPOLAR. THESE EXCEPTIONS ARE THE CHARGE COUPLED DEVICES (CCD) AND THE ERASABLE PROGRAMMABLE READ ONLY MEMORIES (EPROM) WHICH ARE UNIQUELY IMPLEMENTED WITH MOS TECHNOLOGY.

RANDOM ACCESS MEMORIES (RAM) ARE THE FASTEST GROWING SEMICONDUCTOR MEMORIES BECAUSE OF THEIR ABILITY TO REPLACE THE MORE EXPENSIVE CORE MEMORY. ONE OF THE OTHER REASONS FOR THE WIDE ACCEPTANCE IS THE INCREASING BIT DENSITY OF MOS DEVICES. THE DENSITY HAS BEEN QUADRUPLING ON THE AVERAGE OF EVERY TWO YEARS SINCE 1970. THE LEADER IN RAM IS INTEL WHO INTRODUCED THEIR FIRST STATIC MOS RANDOM ACCESS MEMORY IN LATE 1969, IT WAS 256 X 1 BITS. IN 1973 INTEL INTRODUCED THE FIRST 4K DYNAMIC NMOS MEMORY, AND IN 1975 INTEL HAD A PROTOTYPE 16K MEMORY.

THE READ ONLY MEMORY (ROM), LIKE THE RANDOM ACCESS MEMORY, HAS GONE THROUGH EVOLUTIONARY CHANGES IN A SHORT PERIOD OF TIME. INNOVATIONS IN BIPOLAR AND MOS TECHNOLOGY HAVE RESULTED IN PROGRAMMABLE AND ERASABLE PROGRAMMABLE ROM'S, CALLED PROM'S AND EPROM'S RESPECTIVELY. THESE TWO TYPES OF DEVICES HAVE GREATLY INCREASED THE USEFULNESS AND ACCEPTABILITY OF READ ONLY MEMORIES IN SYSTEM APPLICATIONS. READ ONLY MEMORIES ARE NORMALLY MANUFACTURED IN LARGE QUANTITIES USING A MASK PROCESS. THE PROM'S ARE MANUFACTURED AND THEN PROGRAMMED BY BLOWING FUSABLE ELEMENTS OR ALTERING THE ROM STRUCTURE ELECTRICALLY. THE EPROM'S CAN BE

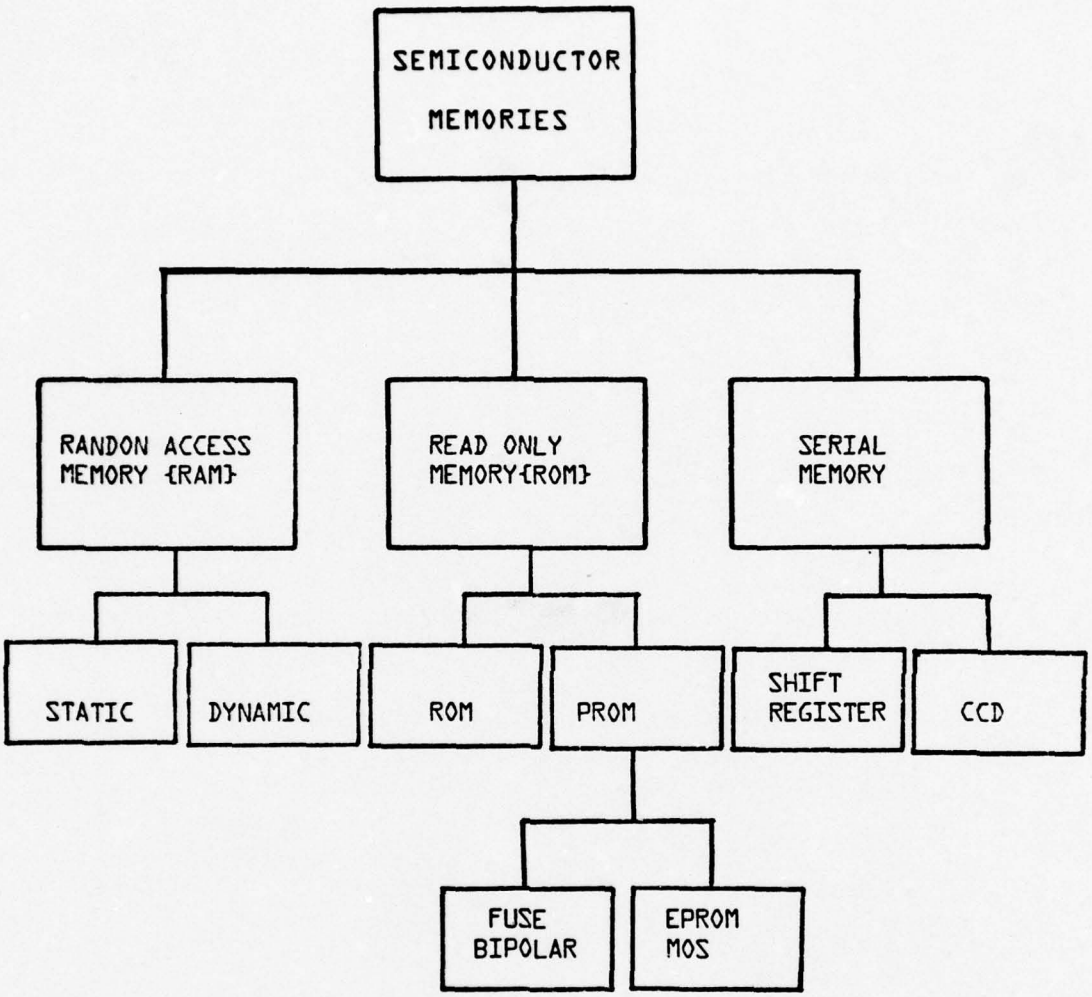

FIGURE 4. SEMICONDUCTOR MEMORY FAMILY TREE

RESTORED TO THEIR UNPROGRAMMED STATE BY EXPOSURE TO ULTRA VIOLET LIGHT. SMALL DEVELOPMENTAL SYSTEMS NORMALLY USE PROM'S AND EPROM'S; WHEREAS, MASS PRODUCTION SYSTEMS USE ROM'S (NON-ALTERABLE OR MASK PROGRAMMABLE).

SERIAL MEMORIES OF EITHER THE SHIFT REGISTER OR CCD TYPE MAKE UP THE HIGH DENSITY AND LOW COST MEMORY SYSTEMS. THEY ARE SUITABLE FOR DRUM REPLACEMENT AS WELL AS OTHER MASS STORAGE APPLICATIONS. FOR EXAMPLE, INTEL ANNOUNCED A MEGA-BIT STORAGE SYSTEM ON A SINGLE PRINTED CIRCUIT CARD IN EARLY 1976.

INTERFACING THE MICROPROCESSOR WITH THE VARIOUS TYPES OF MEMORIES IS VERY STRAIGHT FORWARD WHEN USING THE MOTOROLA 6800. REFERRING TO FIGURE 5, IT IS OBVIOUS THAT THE VARIOUS MEMORY DEVICES ARE SIMPLY CONNECTED TO THE THREE BUSSES. IT SHOULD BE NOTED THAT THE DATA BUS IS IN REALITY EIGHT SPEARATE LINES JUST AS THE ADDRESS BUS IS SIXTEEN LINES. IN OTHER SYSTEMS A SIMILAR BUS STRUCTURE IS USED. THE SIMPLICITY OF THE MOTOROLA BUS IS THE RESULT OF THE DECODER AND DRIVERS BEING LOCATED WITHIN THE ACTIVE CHIPS. IT SHOULD BE NOTED THAT THE BUSSES CAN BE CONNNECTED TO ANY SERIES OF DEVICES SINCE THE MOTOROLA SYSTEM ALLOWS INTERFACING DIRECTLY TO THE MEMORY THROUGH THE BUS STRUCTURE. FIGURE 5 SHOWS TWO TYPES OF INTERFACE ADAPTERS. THE FIRST ADAPTER, KNOWN AS THE PERIPHERAL INTERFACE ADAPTER, ALLOWS TRANSFER OF EIGHT BITS IN PARALLEL TO THE PERIPHERAL DEVICES. {57} THE SECOND DEVICE, THE ASYNCHRONOUS COMMUNICATION ADAPTER, STORES THE EIGHT BITS TEMPORARILY AND TRANSFERS

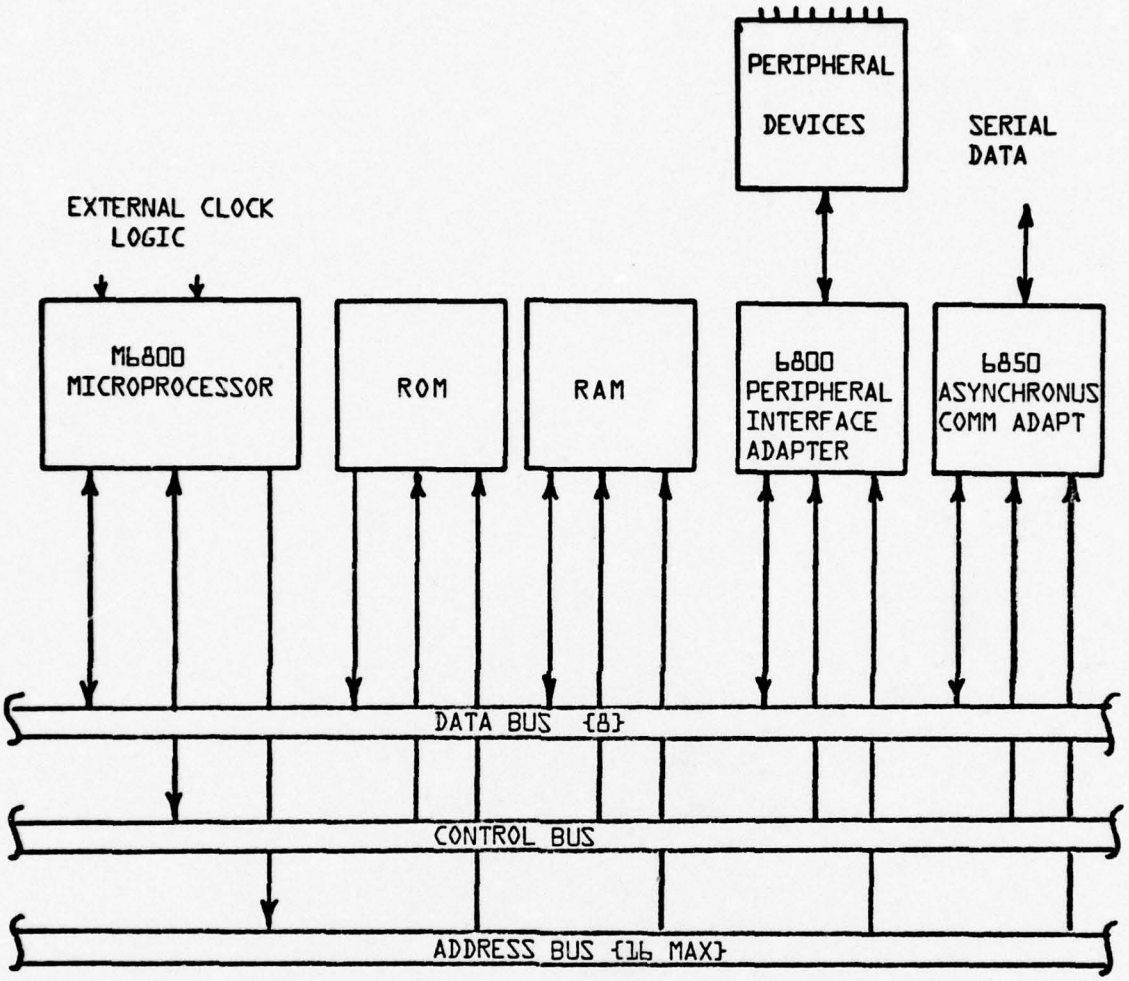

FIGURE 5. THE MOTOROLA M6800 MICROPORSSOR SYSTEM

THE DATA TO A TELETYPEWRITER MACHINE. [35] THESE TWO ADAPTERS CAN TRANSFER INFORMATION INTO THE MICROPROCESSOR AS WELL AS TO THE OUTSIDE WORLD; OBVIOUSLY, IN A MICROPROCESSOR SYSTEM ONLY ONE ACTION OCCURS DURING EACH CLOCK CYCLE.

MICROPROCESSOR SELECTION

NOTWITHSTANDING EARLIER COMMENTS ABOUT THE AGE OF MICROPROCESSORS, ONE SHOULD INSURE THAT A MICROPROCESSOR IS REALLY THE BEST WAY TO GET THE JOB DONE. THERE SHOULD BE A LOGICAL PROCESS FOR SELECTING RANDOM LOGIC OR MICROPROCESSORS. IF DURING THE SYSTEM DESIGN PROCESS, THE DECISION HAS BEEN MADE TO INCORPORATE DIGITAL ELECTRONICS INTO THE DESIGN, THEN ONE SHOULD CONSIDER THE MAGNITUDE OF THE PROBLEM AND THEN THE SPECIFIC DECISION CRITERIA OUTLINED IN THE FLOW DIAGRAM IN FIGURE 6. ASSUMING THAT THE MICROPROCESSOR SOLUTION IS PRACTICAL, THE NEXT STEP IS CONSIDERATION OF THE INPUT/OUTPUT PARAMETERS, HOW LONG IT TAKES TO GET THE DATA PROCESSED, AND SPECIAL CONSTRAINTS SUCH AS SIZE, TEMPERATURE AND COST. ASSUMING THE PROGRAMMABLE PROCESSOR IS THE CHOICE, THERE ARE MANY TYPE AVAILABLE AT MANY LEVELS OF INTEGRATION. THEY RANGE FROM MOS AND BIPOLAR MICROPROCESSOR CHIP SET-UPS, THROUGH MODULAR CARDS, ON UP TO MINICOMPUTERS CONTAINING MICROPROCESSORS. MOST PROCESSORS ARE USED IN FOUR APPLICATION AREAS: DATA ACQUISITION AND CONTROL; DATA COMMUNICATION; HUMAN INTERFACE EQUIPMENT (TERMINALS, POINT-OF-SALE, ETC.); AND COMPUTATION. EACH OF

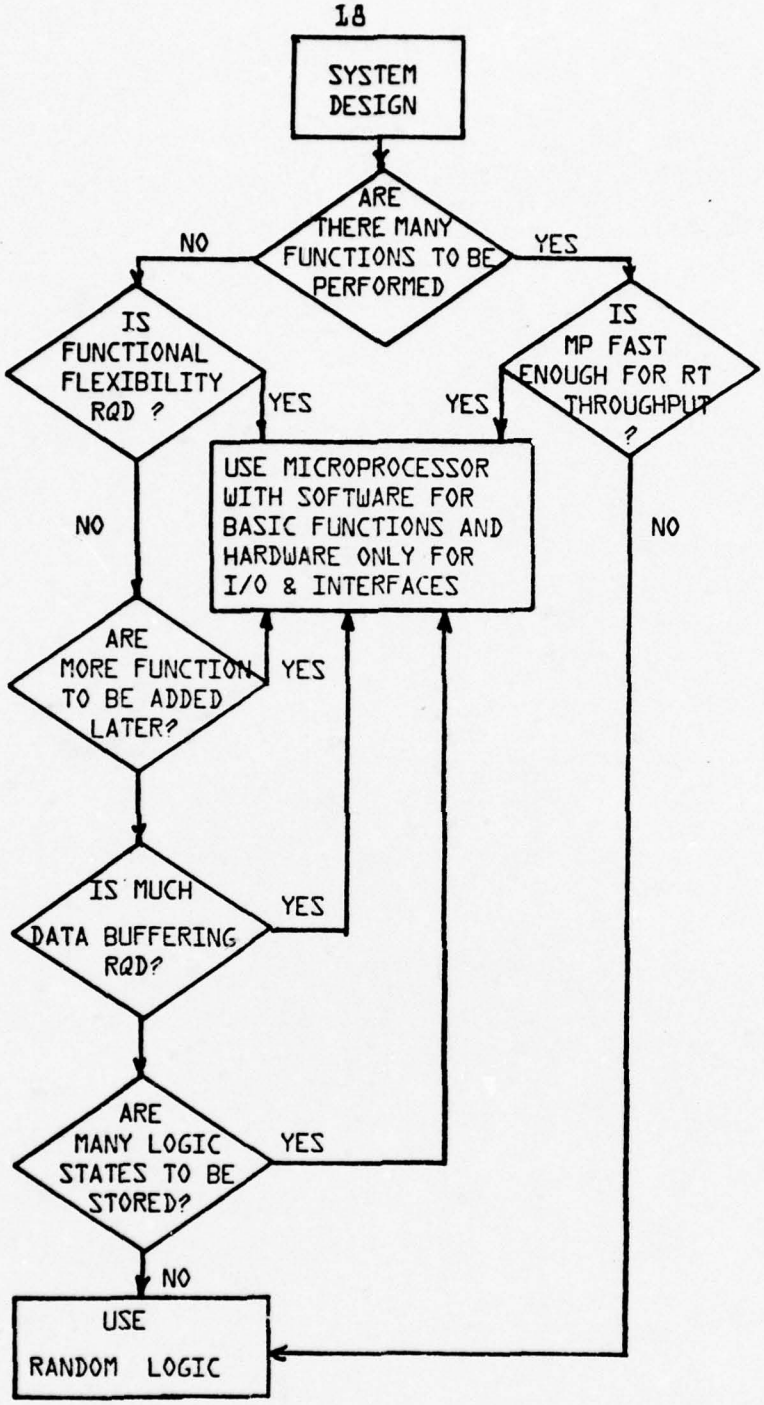

FIGURE 6. MICROPROSSOR VS RANDOM LOGIC DECISION CHART

THESE AREAS STRESSES CERTAIN MICROPROCESSOR CHARACTERISTICS.

FOR DATA ACQUISITION AND CONTROL, THE PROCESSOR SHOULD OFFER: WIDE WORD LENGTH, "NUMBER-CRUNCHING" ABILITY, SPEED, ABILITY TO REACT IN REAL TIME, INTERRUPT CAPABILITY, AND EASE OF INTERFACING WITH ANALOG SIGNAL SOURCES.

FOR DATA COMMUNICATIONS, PRIMARY CHARACTERISTICS ARE: HIGH SPEED DATA HANDLING, GOOD FILE SEARCH, ERROR CODE GENERATION AND CHECKING, AND INTERFACING TO SERIAL DATA LINES. {20,23}

FOR HUMAN INTERFACE, CONSIDERATIONS ARE: LOW COST, SMALL PARTS COUNT, HIGH RELIABILITY, BCD ARITHMETIC CAPABILITIES, LOW SPEED, SOME USER PROGRAMMABILITY, AND SMALL WORD LENGTH.

FOR COMPUTATION, PROCESSOR CAPABILITIES SHOULD INCLUDE: LARGE WORD LENGTH, "NUMBER-CRUNCHING," LOW COST, INTERFACE TO MASS STORAGE, HIGH SPEED, AND HIGHER LEVEL LANGUAGES.

THE INPUT/OUTPUT ANALYSIS CAN BE ACCOMPLISHED BY DETERMINING HOW MANY BIT WIDE THE DATA PATHS ARE, WHAT THE DATA RATE IS, HOW MANY SEPARATE SIGNALS THERE ARE ON THE INPUT TO THE PROCESSOR, ARE THEY SERIAL OR BIT PARALLEL, HOW MANY PERIPHERAL DEVICES MUST BE CONNECTED, CAN THE I/O BE POLLED OR ARE INTERRUPTS REQUIRED, AND FINALLY, IS BLOCK TRANSFER DMA {DIRECT MEMORY ACCESS} NEEDED. WITH THIS ANALYSIS ONE SHOULD CONSULT REFERENCES {14, 33, 38, 39, 45, 47, 49, 52} TO CHOOSE AN APPROPRIATE MICROPROCESSOR SYSTEM.

THE CHOICE OF THE MICROPROCESSOR HARDWARE IS NOT COMPLETE WITHOUT A THOROUGH ANALYSIS OF THE SOFTWARE AVAILABLE FOR THE

MICROPROCESSOR. SOFTWARE IS PROBABLY THE SINGLE MOST IMPORTANT FACTOR IN SYSTEM DESIGN.

SINCE WE ARE IN THE BEGINNING OF "THE AGE OF MICROPROCESSORS" - THE EMPHASIS IS ON THE NEW HARDWARE BEING DEVELOPED. WE ARE JUST STARTING TO PLACE SOME EMPHASIS ON SOFTWARE. FOR EXAMPLE, FEWER THAN TWO HUNDRED PROGRAMS FOR THE INTEL 8080 MICROPROCESSOR ARE ON FILE. IT HAS BEEN ESTIMATED THAT BY 1980, 80% OF THE SYSTEM COST WILL BE SOFTWARE COSTS. CURRENTLY, SOFTWARE COSTS ARE APPROXIMATELY 50%. {18, 26, 34, 53}

THOSE MICROPROCESSOR SYSTEMS WHICH HAVE BEEN FIELDED IN 1975 AND EARLY 1976 AND WHICH ARE SUCCESSFUL ARE THOSE THAT THE DESIGNERS WERE EXTREMELY CAREFUL IN SOFTWARE DEVELOPMENT. {30, 31, 40, 42} THERE HAVE BEEN SEVERAL SYSTEMS FIELDED WHICH HAVE BEEN TOTALLY UNSUCCESSFUL BECAUSE OF SLOPPY SOFTWARE DESIGN. A NEW CONCEPT IN SOFTWARE ANALYSIS HAS BEEN DEVELOPED BY MR. OGDIN. HIS CONCEPT, BRIEFLY, IS TO DEVELOP THE SOFTWARE FROM THE SYSTEM SPECIFICATION; TEST IT ON THE PROTOTYPE HARDWARE; PROVIDE THE SYSTEM SOFTWARE AND HARDWARE TO AN INDEPENDENT AGENCY; AND HAVE THEM DETERMINE THE SYSTEM SPECIFICATION FROM THE SOFTWARE/HARDWARE CONFIGURATION. THIS SPECIFICATION IS THEN COMPARED TO THE ORIGINAL REQUIREMENT AND THE DIFFERENCES NOTED. IF ACCEPTABLE, THE SYSTEM CAN THEN BE PUT INTO PRODUCTION. CHARGES FOR PERFORMING THIS REVERSE ANALYSIS ARE RUNNING IN THE ORDER OF $1 PER BIT FOR MICROPROCESSOR SYSTEMS. THESE COSTS

WILL INCREASE FOR SMALLER SYSTEMS AND DECREASE FOR THE LARGER SYSTEMS. {07}

SINCE WE ARE DISCUSSING COST, IT MIGHT BE INTERESTING TO NOTE WHAT TYPICAL JOBS COST AS OF APRIL 1976. SIMPLE CONTROLLERS AND APPLIANCE CONTROLS WITH ONE OR TWO PACKAGES COST $10. POINT-OF-SALE TERMINALS WITH TEN PACKAGES COST APPROXIMATELY $150. SMART COMMUNICATIONS TERMINALS WITH TEN TO FIFTEEN PACKAGES COST $400. DEDICATED MINICOMPUTERS {MICROPROCESSOR CPU'S} WITH TWENTY TO THIRTY PACKAGES COST $600. NOTE: COST, NOT PRICES, WERE STATED.

MICROPROCESSOR SELECTION CAN BE AIDED BY SENDING ENGINEERS AND MANAGERS TO APPROPRIATE SHORT COURSES OFFERRED BY MANUFACTURERS, UNIVERSITIES, AND PRIVATE CONSULTANTS. APPENDIX C IS A SAMPLE CURRICULUM OFFERED BY A CONSULTANT FIRM. {59} IT IS TYPICAL OF THOSE AVAILABLE AND EMPHASIZES HARDWARE SELECTION AND PROGRAMMING. OTHER SHORT SEMINARS ARE APPLICATIONS ORIENTED AND STRESS MICROPROCESSOR APPLICATION TECHNOLOGY. {19}

APPLICATIONS AND PROJECTED DEVELOPMENTS

TODAY'S APPLICATIONS OF MICROPROCESSORS/MICROCOMPUTERS ARE TILTED HEAVILY TOWARD DATA PROCESSING EQUIPMENT OF VARIOUS KINDS, INCLUDING COMPUTER TERMINALS AND OTHER ACCESSORIES. THE OTHER MAJOR MARKET IS RETAILING EQUIPMENT, I.E., CASH REGISTERS AND POINT-OF-SALE TERMINALS. THE PICTURE IS EXPECTED TO CHANGE WITHIN THE NEXT FEW YEARS AS MICROPROCESSORS INVADE CONSUMER

PRODUCTS IN FORCE. {15} BY 1980 THE CONSUMER PRODUCTS ARE PREDICTED TO ACCOUNT FOR ONE-THIRD OF THE PREDICTED $450 MILLION MICROPROCESSOR MARKET. OTHER MARKETS WILL UNDOUBTEDLY DEVELOP AS INDICATED BY THE FOLLOWING SKETCH. {16}

> THE SERGEANT TURNED TO THE LIEUTENANT AND SAID, "THE ENEMY HAS US SURROUNDED ON ALL SIDES. WHAT SHOULD WE DO?" THE LIEUTENANT ANSWERED, "DON'T WORRY, SARGE, I'VE JUST UNPACKED OUR NEW BATTLEFIELD MICROCOMPUTER, COMPLETE WITH USER INSTRUCTION MANUAL. HEADQUARTERS SAYS IT CAN FIGURE OUT THE BEST SOLUTION TO ANY BATTLEFIELD PROBLEM."
>
> WITHIN A FEW MINUTES, THE BATTLEFIELD MICROCOMPUTER WAS FED THE APPROPRIATE DATA CONCERNING THE DEPLOYMENT OF THE ENEMY. THE LIEUTENANT FED IN THE QUESTION, "WHAT SHOULD WE DO NOW?" IMMEDIATELY, THE LED READOUT ON THE MICROCOMPUTER FLASHED "YES."
>
> THE LIEUTENANT TURNED TO THE SERGEANT AND SAID, "WHAT DOES IT MEAN BY 'YES'?"
>
> THE SERGEANT REPLIED, "MAYBE WE'RE NOT USING IT PROPERLY. INSTEAD OF ASKING IT A QUESTION, WHY DON'T WE GIVE IT A CHOICE OF ANSWERS AND HAVE IT PICK THE BEST ONE?"
>
> THE LIEUTENANT AGREED AND REPHRASED THE INPUT TO THE MICROCOMPUTER AS FOLLOWS. "CONSIDER THE ENEMY FORCE ON OUR LEFT FLANK AS 000, THE ENEMY IN FRONT OF US AS 001, THE ENEMY ON OUR RIGHT FLANK AS 010, AND THE ENEMY IN BACK OF US AS 011. WHICH OF THESE ENEMY POSITIONS SHOULD WE ATTACK?"
>
> ONCE AGAIN, THE COMPUTER FLASHED "YES."
>
> FRUSTRATED, THE LIEUTENANT SCREAMED OUT, "WHAT THE HELL DO YOU MEAN, 'YES'?"
>
> SUDDENLY, THE MICROCOMPUTER SCREEN LIT UP AND FLASHED, "SORRY. YES, SIR." {60}

EVEN THOUGH MICROPROCESSORS HAVE NOT REALLY REACHED THE BATTLEFIELD, THERE ARE MANY PRACTICAL APPLICATIONS FOR THEM. A FEW EXAMPLES OF HIGHLY SUCCESSFUL APPLICATIONS WOULD SERVE TO DEMONSTRATE THE CURRENT STATE OF THE ART IN MICROPROCESSOR TECHNOLOGY.

CHEMETRICS CORPORATION OF BURLINGAME, CALIFORNIA, HAS RECENTLY BROUGHT OUT AN ADVANCED BLOOD CHEMISTRY ANALYZER. ELECTRO UNITS CORPORATION OF SAN JOSE, CALIFORNIA, HAS

DEVELOPED AN ELECTRONIC CONTROL SYSTEM FOR BARS; IT DOLES OUT PRECISELY MEASURED DRINKS AND SERVES AS AN ATTENTIVE INVENTORY CONTROLLER, TOO. TELESENSORY SYSTEM, INC. OF PALO ALTO, CA, HAS INTRODUCED A TALKING CALCULATOR FOR THE BLIND, WITH A RECORDED VOCABULARY OF 24 WORDS FOR SPOKEN VERIFICATION OF CALCULATION STEPS AND RESULTS.

LARGE COMPANIES ARE ALSO TURNING OUT NEW PRODUCTS. GENERAL ELECTRIC RECENTLY INTRODUCED A ROBOT INDUSTRIAL TOOL RUN BY A TINY COMPUTER. AMF, WITH THE AID OF MOTOROLA, DEVELOPED AN AUTOMATIC SCORER FOR USE IN BOWLING ALLEYS. TAPPAN COMPANY HAS DESIGNED A MICROWAVE OVEN WITH TOUCH AND COOK CONTROL USING A SINGLE CHIP MICROCOMPUTER BY TEXAS INSTRUMENT. FORD MOTOR COMPANY HAS DEVELOPED MICROCOMPUTER CONTROLS FOR AUTOMOBILES WHICH REDUCE FUEL CONSUMPTION BY 20% (TO BE INTRODUCED IN THE 1979 MODELS).

SYSTEMS UNDER DEVELOPMENT INCLUDE A RADAR POSITION COORDINATE CONVERTER BY RCA WHICH WILL CONVERT RADAR DATA TO A FIXED REFERENCE COORDINATE SYSTEM. ENVIRONMENT CANADA, FISHERIES AND MARINE SERVICE, IS BUILDING A DIGITAL INTEGRATER TO ENHANCE THE ACCURACY OF ECHO SOUNDERS TO PROVIDE ESTIMATES OF THE HERRING SCHOOLS TO HELP SET HARVEST RATES THAT WILL INSURE THAT ENOUGH FISH REACH THE SPAWNING AREAS TO MAINTAIN THE SPECIES. FROST COMMUNICATIONS IS DEVELOPING A RADIO TELEPHONE SYSTEM USING MICROPROCESSORS FOR CONTROL, SWITCHING AND BILLING. THERE IS ONE MICROPROCESSOR IN EACH MOBILE UNIT AND SEVERAL

USED IN EACH BASE STATION OF THE RADIO TELEPHONE SYSTEM. THIS SYSTEM PERMITS THE MOBILE TELEPHONE TO BE USED AS A CONVENTIONAL TELEPHONE. {05}

ANOTHER AREA NOT PREVIOUSLY MENTIONED THAT ACCOUNTS FOR MANY DEVELOPMENTAL HOURS IS THE APPLICATION OF MICROPROCESSORS TO VIDEO GAMES SUCH AS PING PONG, HANDBALL, SPACE WAR GAMES, AND COWBOYS AND INDIANS. MANY MANUFACTURERS OF PINBALL MACHINES ARE CONVERTING TO THEIR ELECTRONIC COUNTERPARTS TO INCREASE PROFITS BY REDUCING SERVICE CALLS AND MAINTENANCE COSTS. {62}

LOOKING INTO THE FUTURE OF MICROPROCESSORS IS DIFFICULT AT BEST BECAUSE THE APPLICATIONS APPEAR BOUNDLESS AND LIMITED ONLY BY THE IMAGINATION OF MANAGEMENT AND ENGINEERING PERSONNEL. {50} FUTURE HARDWARE DEVELOPMENTS OBVIOUSLY INCLUDE THE REDUCTION OF MEMORY AND I/O PHYSICAL SIZE TO THE POINT WHERE IT IS INCLUDED ON THE CHIP WITH THE MICROPROCESSOR. {63} THIS ONE-CHIP COMPUTER WILL HAVE MANY APPLICATIONS IN THE APPLIANCE/CONTROL AREA. OTHER SIGNIFICANT HARDWARE DEVELOPMENTS WILL INCLUDE THE INCREASE IN SIZE OF THE VARIOUS MEMORIES. THE EVENTUAL REPLACEMENT OF ROTATING STORAGE DEVICES IS INEVITABLE. {29}

WELCOME TO "THE AGE OF MICROPROCESSORS."

APPENDIX A

GLOSSARY OF COMMON WORDS

ACCUMULATOR: ONE OR MORE REGISTERS ASSOCIATED WITH THE ALU WHICH TEMPORARILY STORE SUMS AND OTHER ARITHMETICAL AND LOGICAL RESULTS OF THE ALU.

ACIA {ASYNCHROUS COMMUNICATIONS INTERFACE ADAPTER}: A MOTOROLA DEVICE WHICH INTERFACES THE MICROPROCESSOR'S BUS-ORGANIZED SYSTEM WITH INCOMING SERIAL SYNCHRONOUS COMMUNICATION INFORMATION. THE PARALLEL DATA OF THE MULTI-BUS SYSTEM IS SERIALLY TRANSMITTED BY THE ASYNCHRONOUS DATA TERMINAL. THE ACIA INTERFACES DIRECTLY WITH LOW-SPEED MODEMS TO ENABLE MICROPROCESSOR COMMUNICATION OVER TELEPHONE LINES.

ADDRESSING MODES: AN ADDRESS IS A CODED INSTRUCTION DESIGNATING THE LOCATION OF DATA OR PROGRAM SEGMENTS IN STORAGE. THE ADDRESS MAY REFER TO STORAGE IN REGISTERS OR MEMORIES OR BOTH. THE ADDRESS CODE ITSELF MAY BE STORED SO THAT A LOCATION MAY CONTAIN THE ADDRESS OF DATA RATHER THAN THE DATA ITSELF. THIS FORM OF ADDRESSING IS COMMON IN MICROPROCESSORS. ADDRESSING MODES VARY CONSIDERABLY BECAUSE OF EFFORTS TO REDUCE PROGRAM EXECUTION TIME.

ALU {ARITHMETIC AND LOGIC UNIT}: THE ALU IS ONE OF THE THREE ESSENTIAL COMPONENTS OF A MICROPROCESSOR...THE OTHER TWO BEING THE REGISTERS AND THE CONTROL BLOCK. THE ALU PERFORMS VARIOUS FORMS OF ADDITION AND SUBTRACTION; THE LOGIC MODE PERFORMS SUCH LOGIC OPERATIONS AS ANDING THE CONTENTS OF TWO REGISTERS, OR MASKING THE CONTENTS OF A REGISTER.

ARCHITECTURE; ANY DESIGN OR ORDERLY ARRANGEMENT PERCEIVED BY MAN: THE ARCHITECTURE OF THE MICROPROCESSOR. SINCE THE EXTANT MICROPROCESSORS VARY CONSIDERABLY IN DESIGN, THEIR ARCHITECTURE HAS BECOME A BONE OF CONTENTION AMONG THE SPECIALISTS.

ASSEMBLER PROGRAM: THE ASSEMBLER PROGRAM TRANSLATES MAN READABLE SOURCE STATEMENTS {MNEMONICS} INTO MACHING UNDERSTANDABLE OBJECT CODE.

ASSEMBLY LANGUAGE: A MACHINE ORIENTED LANGUAGE. NORMALLY THE PROGRAM IS WRITTEN AS A SERIES OF SOURCE STATEMENTS USING MNEMONIC SYMBOLS THAT SUGGEST THE DEFINITION OF THE INSTRUCTION AND IS THEN TRANSLATED INTO MACHINE LANGUAGE.

BAUD RATE: A MEASURE OF DATA FLOW. THE NUMBER OF SIGNAL ELEMENTS PER SECOND BASED ON THE DURATION OF THE SHORTEST

ELEMENT. WHEN EACH ELEMENT CARRIES ONE BIT, THE BAUD RATE IS NUMERICALLY EQUAL TO BITS PER SECOND (BPS). THE BAUD RATES ON UART DATA SHEETS ARE INTERCHANGEABLE WITH BPS.

BCD (BINARY CODED DECIMAL): EACH DECIMAL DIGIT IS BINARY CODED INTO 4-BIT WORDS. THE DECIMAL NUMBER 11 WOULD BECOME 0001 0001 IN BCD. ALSO KNOWN AS THE 8421 CODE.

BENCHMARK: ORIGINALLY A SURVEYOR'S MARK USED AS A REFERENCE POINT IN SURVEYS. IN CONNECTION WITH MICROPROCESSORS, THE BENCHMARK IS A FREQUENTLY USED ROUTINE OR PROGRAM SELECTED FOR THE PURPOSE OF COMPARING DIFFERENT MAKES OF MICROPROCESSORS. A FLOW CHART IN ASSEMBLY LANGUAGE IS WRITTEN OUT FOR EACH MICROPROCESSOR AND THE EXECUTION OF THE BENCHMARK BY EACH UNIT IS EVALUATED ON PAPER. IT IS NOT NECESSARY TO USE HARDWARE TO MEASURE CAPABILITY BY BENCHMARK.

BIDIRECTIONAL: A TERM APPLIED TO A PORT OR BUS LINE THAT CAN BE USED TO TRANSFER DATA IN EITHER DIRECTION.

BRANCH: REFERS TO THE CAPABILITY OF A MICROPROCESSOR TO MODIFY THE FUNCTION OR PROGRAM SEQUENCE. SUCH MODIFICATION DEPENDS ON THE ACTUAL CONTENT OF THE DATA BEING PROCESSED AT ANY GIVEN INSTANT.

BUFFER: A CIRCUIT INSERTED BETWEEN OTHER CIRCUIT ELEMENTS TO PREVENT INTERACTIONS, TO MATCH IMPEDANCES, TO SUPPLY ADDITIONAL DRIVE CAPABILITY, OR TO DELAY RATE OF INFORMATION FLOW. BUFFERS MAY BE INVERTING OR NON-INVERTING.

BUS SYSTEM: A NETWORK OF PATHS INSIDE THE MICROPROCESSOR WHICH FACILITATE DATA FLOW. THE IMPORTANT BUSSES IN A MICROPROCESSOR ARE IDENTIFIED AS DATA BUS, ADDRESS BUS, AND CONTROL BUS.

BYTE: INDICATES A PRE-DETERMINED NUMBER OF CONSECUTIVE BITS TREATED AS AN ENTITY. FOR EXAMPLE, 4-BIT OR 8-BIT BYTES. "WORD" AND "BYTE" ARE USED INTERCHANGEABLY.

CLOCK: A GENERATOR OF PULSES WHICH CONTROLS THE TIMING OF SWITCHING CIRCUITS IN A MICROPROCESSOR. CLOCK FREQUENCY IS NOT THE ONLY CRITERION OF DATA MANIPULATION SPEED. HARDWARE ARCHITECTURE AND PROGRAMMING SKILL ARE MORE IMPORTANT. CLOCKS ARE A REQUISITE FOR MOST MICROPROCESSORS AND MULTIPLE PHASED CLOCKS ARE COMMON IN MOS PROCESSORS.

COMPILERS: COMPILERS TRANSLATE HIGHER-LEVEL LANGUAGES INTO MACHINE CODE.

CONTROL BLOCK: THIS IS THE CIRCUITRY WHICH PERFORMS THE CONTROL FUNCTIONS OF THE CPU. IT IS RESPONSIBLE FOR DECODING MICROPROGRAMMED INSTRUCTIONS, AND THEN GENERATING THE INTERNAL CONTROL SIGNALS THAT PERFORM THE OPERATIONS REQUESTED.

CONTROL BUS: CONVEYS A MIXTURE OF SIGNALS WHICH REGULATE SYSTEM OPERATION. THESE "TRAFFIC" SIGNALS ARE COMMANDS WHICH MAY ALSO ORIGINATE IN PERIPHERALS FOR TRANSFER TO THE CPU OR THE REVERSE.

CONTROL PROGRAM: THE CONTROL PROGRAM IS A SEQUENCE OF INSTRUCTIONS THAT WILL GUIDE THE CPU THROUGH THE VARIOUS OPERATIONS IT MUST PERFORM. THIS PROGRAM IS STORED PERMANENTLY IN ROM MEMORY WHERE IT CAN BE ACCESSED BY THE CPU DURING OPERATIONS.

CPU {CENTRAL PROCESSING UNIT}: THE HEART OF ANY COMPUTER SYSTEM. BASICALLY THE CPU IS MADE UP OF STORAGE ELEMENTS CALLED REGISTERS, COMPUTATIONAL CIRCUITS IN THE ALU, THE CONTROL BLOCK, AND I/O. AS SOON AS LSI TECHNOLOGY WAS ABLE TO BUILD A CPU ON AN IC CHIP, THE MICROPROCESSOR BECAME A REALITY. THE ONE-CHIP MICROPROCESSORS HAVE LIMITED STORAGE SPACE, SO MEMORY IMPLEMENTATION IS ADDED IN MODULAR FASHION. MOST CURRENT MICROPROCESSORS CONSIST OF A SET OF CHIPS, ONE OR TWO OF WHICH FORM THE CPU.

CROSS-ASSEMBLER: WHEN THE PROGRAM IS ASSEMBLED BY THE SAME MICROPROCESSOR THAT IT WILL RUN ON, THE PROGRAM THAT PERFORMS THE ASSEMBLY IS REFERRED TO SIMPLY AS AN ASSEMBLER. IF THE PROGRAM IS ASSEMBLED BY SOME OTHER MICROPROCESSOR, THE PROCESS IS REFERRED TO AS CROSS-ASSEMBLY. OCCASIONALLY THE PHRASE "NATIVE ASSEMBLER" WILL BE USED TO DISTINGUISH IT FROM A CROSS-ASSEMBLER.

DAISY CHAIN: A BUS LINE WHICH IS INTERCONNECTED WITH UNITS IN SUCH A WAY THAT THE SIGNAL PASSES FROM ONE UNIT TO THE NEXT IN SERIAL FASHION. THE ARCHITECTURE OF THE FAIRCHILD F-8 PROVIDES AN EXAMPLE OF DAISY-CHAINED MEMORY CHIPS. EACH CHIP CONNECTS TO ITS NEIGHBORS TO ACCOMPLISH DAISY-CHAINING OF INTERRUPT PRIORITIES BEGINNING WITH THE CHIP CLOSEST TO THE CPU.

DATA BUS: THE MICROPROCESSOR COMMUNICATES INTERNALLY AND EXTERNALLY BY MEANS OF THE DATA BUS. IT IS BIDIRECTIONAL AND CAN TRANSFER DATA TO AND FROM THE CPU, MEMORY STORAGE, AND PERIPHERAL DEVICES.

DEBUG: AS USED IN CONNECTION WITH MICROPROCESSOR SOFTWARE, DEBUGGING INVOLVES SEARCHING FOR AND ELIMINATING SOURCES

OF ERROR IN PROGRAMMING ROUTINES. FINDING A BUG IN SOFTWARE ROUTINE IS SAID TO BE AS DIFFICULT AS FINDING A NEEDLE IN THE PROVERBIAL HAYSTACK. A SINGLE STEP TESTER IS THE SUGGESTED METHOD, SO THAT EACH INSTRUCTION OPERATION CAN BE CHECKED INDIVIDUALLY.

DECREMENT: A PROGRAMMING INSTRUCTION WHICH DECREASES THE CONTENTS OF A STORAGE LOCATION. {SEE ALSO INCREMENT AND DECREMENT.}

DEDICATED: TO SET APART FOR SOME SPECIAL USE. A DEDICATED MICROPROCESSOR IS ONE THAT HAS BEEN SPECIFICALLY PROGRAMMED FOR A SINGLE APPLICATION SUCH AS WEIGHT MEASUREMENT BY SCALE, TRAFFIC LIGHT CONTROL, ETC. ROM'S BY THEIR VERY NATURE {READ-ONLY} ARE "DEDICATED" MEMORIES.

DIRECT ADDRESSING: THIS IS THE STANDARD ADDRESSING MODE. IT IS CHARACTERIZED BY AN ABILITY TO REACH ANY POINT IN MAIN STORAGE DIRECTLY. DIRECT ADDRESSING IS SOMETIMES RESTRICTED TO THE FIRST 256 BITS IN MAIN STORAGE.

DMA {DIRECT MEMORY ACCESS}: A METHOD OF GAINING DIRECT ACCESS TO MAIN STORAGE TO ACHIEVE DATA TRANSFER WITHOUT INVOLVING THE CPU. THE MANNER IN WHICH CPU IS DISABLED WHILE DMA IS IN PROGRESS DIFFERS IN DIFFERENT MODELS AND SOME USE SEVERAL METHODS TO ACCOMPLISH DMA.

EXECUTION TIME: USUALLY EXPRESSED IN CLOCK CYCLES NECESSARY TO CARRY OUT AN INSTRUCTION. SINCE THE CLOCK FREQUENCY IS KNOWN, THE ACTUAL TIME CAN BE CALCULATED. CLOCK FREQUENCIES CAN BE VARIED.

EXTENDED ADDRESSING: REFERS TO AN ADDRESSING MODE THAT CAN REACH ANY PLACE IN MEMORY. SEE ALSO DIRECT ADDRESSING.

FETCH: TO GO AFTER AND RETURN WITH THINGS. IN A MICROPROCESSOR, THE "OBJECTS" FETCHED ARE INSTRUCTIONS WHICH ARE ENTERED IN THE INSTRUCTION REGISTER. THE NEXT, OR A LATER STEP IN THE PROGRAM, WILL CAUSE THE MACHINE TO EXECUTE WHAT IT WAS PROGRAMMED TO DO WITH THE FETCHED INSTRUCTIONS. OFTEN REFERRED TO AS AN "INSTRUCTION FETCH."

FIRMWARE: SOFTWARE INSTRUCTIONS WHICH HAVE BEEN PERMANENTLY FROZEN INTO A ROM ARE SOMETIMES REFFERED TO AS FIRMWARE.

FLAG BIT: AN INFORMATION BIT WHICH INDICATES SOME FORM OF DEMARCATION HAS BEEN REACHED SUCH AS OVERFLOW OR CARRY. ALSO AN INDICATOR OF SPECIAL CONDITIONS SUCH AS INTERRUPTS.

FLOW CHART OR FLOW DIAGRAM: A SEQUENCE OF OPERATIONS CHARTED

WITH THE AID OF SYMBOLS, DIAGRAMS, OR OTHER REPRESENTATIONS TO INDICATE AN EXECUTIVE PROGRAM. FLOWCHARTS ENABLE THE DESIGNER TO VISUALIZE THE PROCEDURE NECESSARY FOR EACH ITEM ON THE PROGRAM. A COMPLETE FLOWCHART LEADS DIRECTLY TO THE FINAL CODE.

HANDSHAKING: A COLLOQUIAL TERM WHICH DESCRIBES THE METHOD USED BY A MODEM TO ESTABLISH CONTACT WITH ANOTHER MODEM AT THE OTHER END OF A TELEPHONE LINE. OFTEN USED INTERCHANGEABLY WITH BUFFERING AND INTERFACING, BUT WITH A FINE LINE OF DIFFERENCE IN WHICH HANDSHAKING IMPLIES A DIRECT PACKAGE CONNECTION REGARDLESS OF FUNCTIONAL CIRCUITRY.

HARDWARE: THE INDIVIDUAL COMPONENTS OF A CIRCUIT, BOTH PASSIVE AND ACTIVE, HAVE LONG BEEN CHARACTERIZED AS HARDWARE IN THE JARGON OF THE ENGINEER. TODAY, ANY PIECE OF DATA PROCESSING EQUIPMENT IS INFORMALLY CALLED HARDWARE.

HARD-WIRED LOGIC: RANDOM LOGIC DESIGN SOLUTIONS REQUIRE INTERCONNECTION OF NUMEROUS INTEGRATED CIRCUITS REPRESENTING THE LOGIC ELEMENTS. AN EXAMPLE OF HARD-WIRED LOGIC IS THE USE OF A HAND-WIRED DIODE MATRIX INSTEAD OF A ROM. THESE INTERCONNECTIONS, WHETHER DONE WITH SOLDERING IRON OR BY PRINTED CIRCUIT BOARD, ARE REFERRED TO AS HARD-WIRED LOGIC IN CONTRAST TO THE SOFTWARE SOLUTIONS ACHIEVED BY A PROGRAMMED ROM OR MICROPROCESSOR.

HIGH LEVEL LANGUAGE: THIS IS A PROBLEM-ORIENTED PROGRAMMING LANGUAGE AS DISTINGUISHED FROM A MACHINE-ORIENTED PROGRAMMING LANGUAGE. THE FORMER'S INSTRUCTION APPROACH IS CLOSER TO THE NEEDS OF THE PROBLEMS TO BE HANDLED THAN THE LANGUAGE OF THE MACHINE ON WHICH THEY ARE TO BE IMPLEMENTED.

IMMEDIATE ADDRESSING: IN THIS MODE OF ADDRESSING, THE OPERAND CONTAINS THE VALUE TO BE OPERATED ON, AND NO ADDRESS REFERENCE IS REQUIRED.

INCREMENT (AND DECREMENT): THESE TWO WORDS ARE SOFTWARE OPERATIONS MOST OFTEN ASSOCIATED WITH THE STACK AND STACK POINTER. BYTES OF INFORMATION ARE STORED IN THE STACK REGISTER AT THE ADDRESSES CONTAINED IN THE STACK POINTER. THE STACK POINTER IS DECREMENTED AFTER EACH BYTE OF INFORMATION IS ENTERED INTO THE STACK; IT IS INCREMENTED AFTER EACH BYTE IS REMOVED FROM THE STACK. THE TERMS CAN ALSO REFER TO ANY ADDRESSABLE REGISTER.

INDEX REGISTER: THE INDEX REGISTER CONTAINS ADDRESS INFORMATION SUBJECT TO MODIFICATION BY THE CONTROL BLOCK WITHOUT AFFECTING THE INSTRUCTION IN THE MEMORY. THE IR

INFORMATION IS AVAILABLE FOR LOADING ONTO THE STACK POINTER WHEN NEEDED.

INDIRECT ADDRESSING: ADDRESSING A MEMORY LOCATION WHICH CONTAINS THE ADDRESS OF DATA RATHER THAN THE DATA ITSELF.

INSTRUCTION SET: CONSTITUTES THE TOTAL LIST OF INSTRUCTIONS WHICH CAN BE EXECUTED BY A GIVEN MICROPROCESSOR AND IS SUPPLIED TO THE USER TO PROVIDE THE BASIC INFORMATION NECESSARY TO ASSEMBLE A PROGRAM.

INTERFACE: INDICATES A COMMON BOUNDARY BETWEEN ADJACENT COMPONENTS, CIRCUITS, OR SYSTEMS ENABLING THE DEVICES TO YIELD AND/OR ACQUIRE INFORMATION FROM ONE ANOTHER. IN THE FACE OF COMMON USAGE, ONE MUST REGRETFULLY ADD THAT THE WORDS BUFFER, HANDSHAKE, AND ADAPTER ARE INTERCHANGEABLE WITH INTERFACE.

INTERRUPT: AN INTERRUPT INVOLVES THE SUSPENSION OF THE NORMAL PROGRAMMING ROUTINE OF A MICROPROCESSOR IN ORDER TO HANDLE A SUDDEN REQUEST FOR SERVICE. THE IMPORTANCE OF THE INTERRUPT CAPABILITY OF A MICROPROCESSOR DEPENDS ON THE KIND OF APPLICATIONS TO WHICH IT WILL BE EXPOSED. WHEN A NUMBER OF PERIPHERAL DEVICES INTERFACE THE MICROPROCESSOR, ONE OR SEVERAL SIMULTANEOUS INTERRUPTS MAY OCCUR ON A FREQUENT BASIS. MULTIPLE INTERRUPT REQUESTS REQUIRE THE PROCESSOR TO BE ABLE TO ACCOMPLISH THE FOLLOWING: TO DELAY OR PREVENT FURTHER INTERRUPTS; TO BREAK INTO AN INTERRUPT IN ORDER TO HANDLE A MORE URGENT INTERRUPT; TO ESTABLISH A METHOD OF INTERRUPT PRIORITIES; AND, AFTER COMPLETION OF INTERRUPT SERVICE, TO RESUME THE INTERRUPTED PROGRAM FROM THE POINT WHERE IT WAS INTERRUPTED.

INTERRUPT MASK BIT: THE INTERRUPT MASK BIT PREVENTS THE CPU FROM RESPONDING TO FURTHER INTERRUPT REQUESTS UNTIL CLEARED BY EXECUTION OF PROGRAMMED INSTRUCTIONS. IT MAY ALSO BE MANIPULATED BY SPECIFIC MASK BIT INSTRUCTIONS.

I/O {INPUT/OUTPUT}: PACKAGE PINS WHICH ARE TIED DIRECTLY TO THE INTERNAL BUS NETWORK TO ENABLE I/O TO INTERFACE THE MICROPROCESSOR WITH THE OUTSIDE WORLD.

JUMP: THE JUMP OPERATION, LIKE THE BRANCH OPERATION IS USED TO CONTROL THE TRANSFER OF OPERATIONS FROM ONE POINT TO A MORE DISTANT POINT IN THE CONTROL PROGRAM. JUMPS DIFFER FROM BRANCHING IN NOT USING THE RELATIVE ADDRESSING MODE.

LABEL: A LABEL MAY CORRESPOND TO A NUMERICAL VALUE OR A MEMORY LOCATION IN THE PROGRAMMABLE SYSTEM. THE SPECIFIC ABSOLUTE ADDRESS IS NOT NECESSARY SINCE THE INTENT OF THE

LABEL IS A GENERAL DESTINATION. LABELS ARE A REQUISITE FOR JUMP AND BRANCH INSTRUCTIONS.

LIFO: LAST-IN-FIRST-OUT BUFFER. {SEE PUSH DOWN STACK.}

LOGIC: A MATHEMATICAL TREATMENT OF FORMAL LOGIC IN WHICH A SYSTEM OF SYMBOLS IS USED TO REPRESENT QUANTITIES AND RELATIONSHIPS. THE SYMBOLS OR LOGICAL FUNCTIONS ARE CALLED AND, OR, NOT, TO MENTION A FEW EXAMPLES. EACH FUNCTION CAN BE TRANSLATED INTO A SWITCHING CIRCUIT, MORE COMMONLY REFERRED TO AS A "GATE." SINCE A SWITCH {OR GATE} HAS ONLY TWO STATES - OPEN OR CLOSED - IT MAKES POSSIBLE THE APPLICATION OF BINARY NUMBERS FOR THE SOLUTION OF PROBLEMS. THE BASIC LOGIC FUNCTIONS OBTAINED FROM GATE CIRCUITS IS THE FOUNDATION OF COMPLEX COMPUTING MACHINES.

LOOPING: REPETITION OF INSTRUCTIONS AT DELAYED SPEEDS UNTIL A FINAL VALUE IS DETERMINED {AS IN A WEIGHT SCALE INDICATION} IS CALLED LOOPING. THE LOOPED REPETITIONS ARE USUALLY FROZEN INTO A ROM MEMORY LOCATION AND THEN JUMPED TO WHEN NEEDED. LOOPING ALSO OCCURS WHEN THE CPU IS IN A WAIT CONDITION.

LSI {LARGE SCALE INTEGRATION}: AT THE BEGINNING OF THE LSI ERA A COUNT OF 100 GATES QUALIFIED FOR LSI. TODAY AN 8-BIT CPU CAN BE FABRICATED ON A SINGLE CHIP.

MACHINE LANGUAGE: THE ONLY LANGUAGE THE MICROPROCESSOR CAN UNDERSTAND IS BINARY. ALL OTHER PROGRAMMING LANGUAGES MUST BE TRANSLATED INTO BINARY CODE BEFORE ENTERING THE PROCESSOR AND DECODED BACK INTO THE ORIGINAL LANGUAGE AFTER LEAVING IT.

MAIL BOX: THE MAIL BOX IS A SET OF LOCATIONS IN A COMMON RAM STORAGE AREA RESERVED FOR DATA ADDRESSED TO SPECIFIC PERIPHERAL DEVICES AS WELL AS OTHER MICROPROCESSORS IN THE IMMEDIATE ENVIRONMENT. SUCH AN ARRANGEMENT ENABLES THE CO-ORDINATOR CPU AND THE SUPPLEMENTARY MICROPROCESSORS TO TRANSFER DATA AMONG THEMSELVES IN AN ORDERLY FASHION WITH MINIMAL HARDWAR.

MICROPROGRAM: THIS WORD PRE-DATES THE MICROPROCESSOR AND REFERS TO COMPUTER INSTRUCTIONS WHICH DO NOT REFERENCE THE MAIN MEMORY STORAGE. IT IS A COMPUTER TECHNIQUE WHICH PERFORMS SUBROUTINES BY MANIPULATING THE BASIC COMPUTER HARDWARE AND IS OFTEN REFERRED TO AS "COMPUTER WITHIN COMPUTER." THE WORD HAS NOT CHANGED ITS BASIC MEANING WHEN USED IN CONNECTION WITH MICROPROCESSORS, BUT IS NOT TO BE CONSTRUED AS NATIVE TO MICROPROCESSORS. A SERIES OF INSTRUCTIONS STORED IN A ROM, ANY PORTION OF WHICH CAN IMPLEMENT

A HIGHER LANGUAGE PROGRAM, IS LABELED A MICROPROGRAM.

MEMORY: THE PART OF A COMPUTER SYSTEM INTO WHICH INFORMATION CAN BE INSERTED AND HELD FOR FUTURE USE. STORAGE AND MEMORY ARE INTERCHANGEABLE EXPRESSIONS. MEMORIES ACCEPT AND HOLD BINARY NUMBERS ONLY. MEMORY TYPES ARE CORE, DISK, DRUM, AND SEMICONDUCTOR.

MOS {METAL OXIDE SEMICONDUCTOR}: THE STRUCTURE OF AN MOS FIELD EFFECT TRANSISTOR {FET} IS METAL OVER SILICON OXIDE OVER SILICON. THE METAL ELECTRODE IS THE GATE; THE SILICON OXIDE IS THE INSULATOR; AND CARRIER DOPED REGIONS IN THE SILICON SUBSTRATE BECOME THE DRAIN AND SOURCE. THE RESULT IS A SNADWICH VERY MUCH LIKE A CAPACITOR, WHICH EXPLAINS WHY MOS IS SLOWER THAN BIPOLAR SINCE THE "CAPACITOR SANDWICH" MUST CHARGE UP BEFORE CURRENT CAN FLOW. THE THREE GREAT ADVANTAGES OF MOS ARE ITS PROCESS SIMPLICITY BECAUSE OF REDUCED FABRICATION STAGES; THE SAVINGS IN CHIP REAL ESTATE RESULTING IN FUNCTIONAL DENSITY; AND THE EASE OF INTERCONNECTION ON CHIP. THESE QUALITIES ENABLED MOS TO BREAK THE LSI BARRIER, SOMETHING BIPOLAR IS JUST BEGINNING TO ACHIEVE. THE HAND-HELD CALCULATOR AND THE MICROPROCESSOR ARE TRIUMPHS OF MOS-LSI TECHNOLOGY.

MICROPROCESSOR: THE MICROPROCESSOR IS A CENTRAL PROCESSING UNIT FABRICATED ON ONE OR TWO CHIPS. WHILE NO STANDARD DESIGN IS VISIBLE IN EXISTING UNITS, A NUMBER OF WELL-DELINEATED AREAS ARE PRESENT IN ALL OF THEM: ARITHMETIC & LOGIC UNIT, CONTROL BLOCK, AND REGISTER ARRAY. WHEN JOINED TO A MEMORY STORAGE SYSTEM, THE RESULTING COMBINATION IS REFERRED TO IN TODAY'S USAGE AS A MICROPROCESSOR. IT SHOULD BE ADDED THAT EACH MICROPROCESSOR IS SUPPLIED WITH AN INSTRUCTION SET, AND THIS SOFTWARE MANUAL MAY BE JUST AS IMPORTANT TO THE USER AS THE HARDWARE.

MULTIPLEXING: MULTIPLEXING DESCRIBES A PROCESS OF TRANSMITTING MORE THAN ONE SIGNAL AT A TIME OVER A SINGLE LINK, ROUTE, OR CHANNEL. OF THE TWO METHODS IN USE, ONE FREQUENCY-SHARES THE BANDWIDTH OF A CHANNEL IN THE SAME WAY HURDLERS RUN AND JUMP IN THEIR ASSIGNED LANES THUS PERMITTING MANY CONTESTANTS TO COMPETE SIMULTANEOUSLY ON THE SAME TRACK. THE SECOND WAY IS TO TIME-SHARE MULTIPLE SIGNALS IN THE SAME WAY POLE VAULTERS JUMP OVER THE SAME BAR ONE AFTER THE OTHER. THE TWO METHODS MAY BE DESCRIBED AS PARALLEL AND SERIAL PROCESSING. TIME-SHARING MAY NOT SEEM "SIMULTANEOUS," BUT IT SHOULD BE REMEMBERED THAT THE SIGNAL SPEED IS SO FAST THAT IT IS POSSIBLE TO MULTIPLEX FOUR DIFFERENT NUMBERS THROUGH A SINGLE DECODER-DRIVER AND HAVE THEM APPEAR ON FOUR DIFFERENT DISPLAYS WITHOUT A FLICKER TO DISTURB THE EYE.

OBJECT PROGRAM: THE END RESULT OF THE SOURCE LANGUAGE PROGRAM AFTER IT HAS BEEN TRANSLATED INTO MACHINE LANGUAGE.

OPERAND: A QUANTITY ON WHICH A MATHEMATICAL OPERATION IS PERFORMED. ONE OF THE INSTRUCTION FIELDS IN AN ADDRESSING STATEMENT. USUALLY THE STATEMENT CONSISTS OF AN OPERATOR AND AN OPERAND. THE OPERATOR MAY INDICATE AN "ADD" INSTRUCTION; THE OPERAND WILL INDICATE WHAT IS TO BE ADDED.

OVERFLOW: OVERFLOW RESULTS WHEN AN ARITHMETIC OPERATION GENERATES A QUANTITY BEYOND THE CAPACITY OF THE REGISTER. ALSO REFERRED TO AS ARITHMETICAL OVERFLOW. AN OVERFLOW STATUS BIT IN THE CONDITION CODE REGISTER CAN BE CHECKED TO DETERMINE IF THE PREVIOUS OPERATION CAUSED THE OVERFLOW.

OPERATING CODE (OPCODE): SOURCE STATEMENTS WHICH GENERATE MACHINE CODES AFTER ASSEMBLY ARE REFERRED TO AS OPERATING CODES.

PARALLEL OPERATION: PROCESSING ALL THE DIGITS OF A WORD OR BYTE SIMULTANEOUSLY BY TRANSMITTING EACH DIGIT ON A SEPARATE CHANNEL OR BUS LINE.

PARTY-LINE: PARTY-LINE AS USED IN ITS TELEPHONE SENSE TO INDICATE A LARGE NUMBER OF DEVICES CONNECTED TO A SINGLE LINE ORIGINATING IN THE CPU.

POLLING: POLLING IS THE METHOD USED TO IDENTIFY THE SOURCE OF INTERRUPT REQUESTS. WHEN SEVERAL INTERRUPTS OCCUR AT ONE TIME, THE CONTROL PROGRAM DECIDES WHICH ONE TO SERVICE FIRST.

PORT: DEVICE TERMINALS WHICH PROVIDE ELECTRICAL ACCESS TO A SYSTEM OR CIRCUIT. THE POINT AT WHICH THE I/O IS IN CONTACT WITH THE OUTSIDE WORLD.

PROGRAM: A PROCEDURE FOR SOLVING A PROBLEM AND FREQUENTLY REFERRED TO AS SOFTWARE.

PROGRAM COUNTER: ONE OF THE REGISTERS IN THE CPU WHICH HOLDS ADDRESSES NECESSARY TO STEP THE MACHINE THROUGH THE PROGRAM. DURING INTERRUPTS, THE PROGRAM COUNTER SAVES THE ADDRESS OF THE INSTRUCTION. BRANCHING ALSO REQUIRES LOADING OF THE RETURN ADDRESS IN THE PROGRAM COUNTER.

PUSH DOWN STACK: A REGISTER THAT RECEIVES INFORMATION FROM THE PROGRAM COUNTER AND STORES THE ADDRESS LOCATIONS OF THE INSTRUCTIONS WHICH HAVE BEEN PUSHED DOWN DURING AN INTERRUPT. THIS STACK CAN BE USED FOR SUBROUTINING. ITS SIZE DETERMINES THE LEVEL OF SUBROUTINE NESTING

(ONE LESS THAN ITS SIZE OR 15 LEVELS OF SUBROUTINE NESTING IN A 16 WORD REGISTER.) WHEN INSTRUCTIONS ARE RETURNED THEY ARE POPPED BACK ON A LAST-IN-FIRST-OUT (LIFO) BASIS.

RAM (RANDOM ACCESS MEMORY): RANDOM IN THE SENSE OF PROVIDING ACCESS TO ANY STORAGE LOCATION POINT IN THE MEMORY IMMEDIATELY BY MEANS OF VERTICAL AND HORIZONTAL CO-ORDINATES. INFORMATION MAY BE "WRITTEN" IN OR "READ" OUT IN THE SAME RAPID WAY.

RANDOM LOGIC DESIGN: DESIGNING A SYSTEM USING DISCRETE LOGIC CIRCUITS. NUMEROUS GATES ARE REQUIRED TO IMPLEMENT THE LOGIC EQUATIONS UNTIL THE PROBLEM IS SOLVED. EVEN THEN, THE DESIGN IS NOT COMPLETED UNTIL ALL REDUNDANT GATES ARE WEEDED OUT. RANDOM LOGIC DESIGN IS NO GUARANTEE OF OPTIMUM GATE COUNT.

REAL TIME OPERATION: DATA PROCESSING TECHNIQUE USED TO ALLOW THE MACHINE TO UTILIZE INFORMATION AS IT BECOMES AVAILABLE, AS OPPOSED TO BATCH PROCESSING AT A TIME UNRELATED TO THE TIME THE INFORMATION WAS GENERATED.

REGISTER: A REGISTER IS A MEMORY ON A SMALLER SCALE. THE WORDS STORED THEREIN MAY INVOLVE ARITHMETICAL, LOGICAL, OR TRANSFERRAL OPERATIONS. STORAGE IN REGISTERS MAY BE TEMPORARY, BUT EVEN MORE IMPORTANT IS THEIR ACCESSIBILITY BY THE CPU. THE NUMBER OF REGISTERS IN A MICROPROCESSOR IS CONSIDERED ONE OF THE MOST IMPORTANT FEATURES OF ITS ARCHITECTURE.

ROM (READ ONLY MEMORY): IN ITS VIRGIN STATE THE ROM CONSISTS OF A MOSAIC OF UNDIFFERENTIATED CELLS. ONE TYPE OF ROM IS PROGRAMMED BY MASK PATTERN AS PART OF THE LAST MANUFACTURING STAGE. ANOTHER, MORE POPULAR TYPE BETTER KNOWN AS P/ROM, IS PROGRAMMABLE IN THE FIELD WITH THE AID OF PROGRAMMER EQUIPMENT. PROGRAM DATA STORED IN ROM'S ARE OFTEN CALLED FIRMWARE BECAUSE THEY CANNOT BE ALTERED. HOWEVER, ANOTHER TYPE OF P/ROM IS NOW ON THE MARKET CALLED EPROM WHICH IS ERASIBLE BY ULTRA VIOLET IRRADIATION AND ELECTRICALLY REPROGRAMMABLE.

SCRATCHPAD: THIS TERM IS APPLIED TO INFORMATION WHICH THE PROCESSING UNIT STORES OR HOLDS TEMPORARILY. IT IS A MEMORY CONTAINING SUBTOTALS FOR VARIOUS UNKNOWNS WHICH ARE NEEDED FOR FINAL RESULTS.

SOFTWARE: WHAT SHEET MUSIC IS TO THE PIANO, SOFTWARE IS TO THE COMPUTER. LOOKED AT FROM A PRACTICAL POINT OF VIEW, ONE MIGHT SAY THAT SOFTWARE IS THE COMPUTER'S INSTRUCTION MANUAL. THE NAME, SOFTWARE, WAS OBVIOUSLY CHOSEN TO

CONTRAST WITH THE FORMIDABLE HARDWARE WHICH CONFRONTED THE FIRST PROGRAMMERS. SOFTWARE IS THE LANGUAGE USED BY A PROGRAMMER TO COMMUNICATE WITH THE COMPUTER. SINCE THE ONLY LANGUAGE SPOKEN BY A COMPUTER IS MATHEMATICAL, THE PROGRAMMER MUST CONVERT HIS VERBAL INSTRUCTIONS INTO NUMBERS. IN THE CASE OF MICROPROCESSORS, WHICH VARY FROM MAKER TO MAKER, SOFTWARE LIBRARIES ARE ASSEMBLED BY THE MANUFACTURER FOR THE BENEFIT OF THE USER.

SOURCE STATEMENT: A PROGRAM WRITTEN IN OTHER THAN MACHINE LANGUAGE, USUALLY IN THREE-LETTER MNEMONIC SYMBOLS, THAT SUGGEST THE DEFINITION OF THE INSTRUCTION. THERE ARE TWO KINDS OF SOURCE STATEMENTS: "EXECUTIVE INSTRUCTIONS" WHICH TRANSLATE INTO OPERATING MACHINE CODE (OPCODE); AND "ASSEMBLY DIRECTIVES" WHICH ARE USEFUL IN DOCUMENTING THE SOURCE PROGRAM, BUT GENERATE NO CODE.

SIMULATOR: A SPECIAL PROGRAM THAT SIMULATES THE LOGICAL OPERATION OF THE MICROPROCESSOR. IT IS DESIGNED TO EXECUTE OBJECT PROGRAMS GENERATED BY A CROSS-ASSEMBLER ON A MACHINE OTHER THAN THE ONE BEING WORKED ON AND IS USEFUL FOR CHECKING AND DEBUGGING PROGRAMS PRIOR TO COMMITTING THEM TO ROM FIRWARE.

STACK: THE STACK IS A BLOCK OF SUCCESSIVE MEMORY LOCATIONS WHICH IS ACCESSIBLE FROM ONE END ON A LAST-IN-FIRST-OUT BASIS (LIFO). THE STACK IS CO-ORDINATED WITH THE STACK POINTER WHICH KEEPS TRACK OF STORAGE AND RETRIEVAL OF EACH BYTE OF INFORMATION IN THE STACK. A STACK MAY BE ANY BLOCK OF SUCCESSIVE INFORMATION LOCATIONS IN THE READ/WRITE MEMORY.

SLICE: A TYPE OF CHIP ARCHITECTURE WHICH PERMITS THE CASCADING OR STACKING OF DEVICES TO INCREASE WORD BIT SIZE.

STACK POINTER: THE STACK POINTER IS CO-ORDINATED WITH THE STORING AND RETRIEVAL OF INFORMATION IN THE STACK. THE STACK POINTER IS DECREMENTED BY ONE IMMEDIATELY FOLLOWING THE STORAGE IN THE STACK OF EACH BYTE OF INFORMATION. CONVERSELY, THE STACK POINTER IS INCREMENTED BY ONE IMMEDIATELY BEFORE RETRIEVING EACH BYTE OF INFORMATION FROM THE STACK. THE STACK POINTER MAY BE MANIPULATED FOR TRANSFERRING ITS CONTENTS TO THE INDEX REGISTER OR VICE VERSA.

STORAGE WORD REGISTER: A GROUP OF BINARY NUMBERS WHICH INFORMS THE USER OF THE PRESENT CONDITION OF THE MICROPROCESSOR. IN THE FAIRCHILD F8, THE STATUS REGISTER PROVIDES THE FOLLOWING FIVE PIECES OF INFORMATION: PLUS OR MINUS SIGN OF THE VALUE IN ACCUMULATOR, OVERFLOW INDICATION, CARRY

BIT, ALL ZERO'S IN ACCUMULATOR, AND INTERRUPT BIT STATUS.

STORAGE: THE WORD STORAGE IS USED INTERCHANGEABLY WITH MEMORY. IN FACT, IT HAS BEEN RECOMMENDED AS THE PREFERRED TERM BY PEOPLE WHO WOULD RATHER NOT IMPLY THAT THE COMPUTER HAS ANY RELATIONSHIP WITH THE HUMAN BRAIN.

SUBROUTINE: PART OF A MAST ROUTINE WHICH MAY BE USED AT WILL IN A VARIETY OF MASTER ROUTINES. THE OBJECT OF A BRANCH OR JUMP COMMAND.

THROUGHPUT: THE SPEED WITH WHICH PROBLEMS OR SEGMENTS OF PROBLEMS ARE PERFORMED IS CALLED THROUGHPUT. DEFINED IN THIS WAY, IT IS OBVIOUS THAT THROUGHPUT WILL VARY FROM APPLICATION TO APPLICATION. AS AN INDEX OF SPEED, THROUGHPUT IS MEANINGFUL ONLY IN TERMS OF YOUR OWN APPLICATION.

UART {UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER}: THIS DEVICE WILL INTERFACE A WORD PARALLEL CONTROLLER OR DATA TERMINAL TO A BIT SERIAL COMMUNICATION NETWORK.

VECTOR INTERRUPT: THIS TERM IS USED TO DESCRIBE A MICROPROCESSOR SYSTEM IN WHICH EACH INTERRUPT, BOTH INTERNAL AND EXTERNAL, HAVE THEIR OWN UNIQUELY RECOGNIZABLE ADDRESS. THIS ENABLES THE MICROPROCESSOR TO PERFORM A SET OF SPECIFIED OPERATIONS WHICH ARE PRE-PROGRAMMED BY THE USER TO HANDLE EACH INTERRUPT IN A DISTINCTIVELY DIFFERENT MANNER.

WORD: A GROUP OF "CHARACTERS" TREATED AS A UNIT AND GIVEN A SINGLE LOCATION IN COMPUTER MEMORY. PRESUMABLY A BYTE IS A GROUP OF BITS IN CONTRAST TO A WORD WHICH IS A GROUP OF NUMERIC AND/OR ALPHABETIC CHARACTERS AND SYMBOLS, BUT THE TWO WORDS ARE USED INTERCHANGEABLY MORE OFTEN THAN NOT.

APPENDIX B

LIST OF MICROPROCESSOR COMPANIES

AEG-TELEFUNKEN, 6 FRANKFURT 70, AEG-HOCHHAUS, GERMANY.

ADAPTIVE SYSTEMS, P.O. BOX 1481, POMPANO BEACH, FL 33061. (305) 942-4000.

ADVANCED MEMORY SYSTEMS, 1275 HAMMERWOOD, SUNNYVALE, CA 94086. (408) 734-4330.

ADVANCED MICRO DEVICES, 901 THOMPSON PL., SUNNYVALE, CA 94086. (408) 732-2400.

AMERICAN MICROSYSTEMS, 3800 HOMESTEAD RD., SANTA CLARA, CA 95051. (408) 246-0330.

APPLIED COMPUTING TECHNOLOGY, 17961 SKY PARK CIRCLE, IRVINE, CA 92707. (714) 557-9972.

BURROUGHS, P.O. BOX 517, PAOLI, PA 19301. (215) 648-2000.

COMPUTER AUTOMATION, 18651 VON KARMAN AVE., IRVINE, CA 92664. (714) 833-8830.

COMSTAR MICROCOMPUTERS, WARNER & SWASEY, 30300 SOLON INDUSTRIAL PKWY., SOLON, OH 44139. (216) 368-6200.

DATA WORKS, 9748 COZYCROFT AVE., CHATSWORTH, CA 91311. (213) 998-8985.

DIGITAL EQUIPMENT CORP., 146 MAIN ST., MAYNARD, MA 01754. (617) 897-5111.

EAGLE SIGNAL INDUSTRIAL CONTROLS DIV., GULF AND WESTERN, 736 FEDERAL ST., DAVENPORT, IA 52803. (319) 326-8101.

ELECTRONIC ARRAYS, 550 E. MIDDLEFIELD RD., MOUNTAIN VIEW, CA 94043. (415) 964-4321.

ESSEX INTERNATIONAL, 564 ALPHA DR., PITTSBURGH, PA 15238. (412) 782-0200.

FAIRCHILD SEMICONDUCTOR, 1725 TECHNOLOGY DR., SAN JOSE, CA 95110. (408) 998-0123.

FUJITSU, 2-CHOME 6-1, CHIYODA-KU TOLYO, JAPAN.

GENERAL AUTOMATION, 1055 S. EAST ST., ANAHEIM, CA 92803. (714) 778-4800.

GENERAL INSTRUMENT, 600 W. JOHN ST., HICKSVILLE, NY 11802. (516) 733-3000.

HARRIS SEMICONDUCTOR, P.O. BOX 883, MELBOURNE, FL 32901. (305) 727-5407.

HITACHI, 23-15 6-CHOME, MINAMIOHI, SHINAGAWA-KU, JAPAN.

INTEL, 3065 BOWERS AVE., SANTA CLARA, CA 95051. (408) 246-7501.

INTERSIL, 10900 N. TANTAU AVE., CUPERTINO, CA 95014. (408) 257-5450.

MARTIN RESEARCH, 1825 S. HALSTED ST., CHICAGO, IL 60608. (312) 829-6932.

MICROCOMPUTER ASSOCIATES, P.O. BOX 304, CUPERTINO, CA 95014. (408) 226-3191.

MITS, 6328 LINN AVE., ALBUQUERQUE, NM 87108. (505) 265-7553.

MONROE CALCULATOR CO., 550 CENTRAL AVE., ORANGE, NJ 07051. (201) 673-6600.

MOS TECHNOLOGY, 950 RITTENHOUSE RD., NORRISTOWN, PA 19401. (215) 666-7950.

MOSTEK, 1215 W. CROSBY RD., CARROLLTON, TX 75006. (214) 242-0444.

MOTOROLA SEMICONDUCTOR, 5005 E. MCDOWELL RD., PHOENIX, AZ 85036. (602) 244-3465.

MULTISONICS, 3300 CROW CANYON RD., P.O. BOX 350, SAN RAMON, CA 94583. (415) 837-8111.

NEC MICROCOMPUTERS, 5 MILITIA DR., LEXINGTON, MA 02173. (617) 862-6410.

NATIONAL SEMICONDUCTOR, 2900 SEMICONDUCTOR DR., SANTA CLARA, CA 95051. (408) 732-5000.

PANAFACOM, P.O. BOX 4637, MOUNTAIN VIEW, CA 94040.

PLESSEY MICROSYSTEMS, 1674 MCGAW AVE., SANTA ANA, CA 92705. (714) 540-9979.

PROCESS COMPUTERS SYSTEMS, 5467 HILL 23 DR., FLINT, MI 48507. (313) 767-8920.

PRO-LOG, 852 AIRPORT RD., MONTEREY, CA 93940. (408) 372-4593.

RCA, ROUTE 202, SOMERVILLE, NJ 08876. (201) 722-3200.

ROCKWELL INTERNATIONAL, MICROELECTRONIC DEVICE DIV., P.O. BOX 3669, ANAHEIM, CA 92803. (714) 632-2321.

SEMI, DIV. OF EM&M, 3883 N. 28 AVE., PHOENIX, AZ 85017. (602) 263-0202.

SIGNETICS, 811 E. ARQUES AVE., SUNNYVALE, CA 94086. (408) 739-7700.

SYNERTEK, 3050 CORONADO DR., SANTA CLARA, CA 95051. (408) 241-4300.

TELEDYNE SYSTEMS, 19601 N. NORDHOFF ST., NORTHBRIDGE, CA 91324. (213) 886-2211.

TEXAS INSTRUMENTS, P.O. BOX 1443, HOUSTON, TX 77001. (713) 494-5115.

TOSHIBA TRANSISTOR WORKS, 1-KOMUKAI, TOSHIBA-CHO, KAWASAKI-CHI, JAPAN.

WESTERN DIGITAL, 19242 RED HILL AVE., NEWPORT BEACH, CA 92663. (714) 557-3550.

ZILOG, 170 STATE ST., LOS ALTOS, CA 94022. (415) 941-5055.

APPENDIX C

EDUCATION COURSES ON MICROPROCESSORS TYPICALLY INCLUDE SUBJECTS AS LISTED BELOW. COSTS ARE FROM $295 TO $495. FOR TWO TO FIVE DAYS.

INTRODUCTION TO MICROPROCESSORS
- THE CPU/ALU
- MEMORY SYSTEM
- CONTROL UNIT
- INPUT/OUTPUT STRUCTURE

MEMORY ORGANIZATION
- PROGRAM AND DATA MEMORIES

REGISTER SYSTEM
- INSTRUCTION AND DATA WORDS, PROGRAM COUNTER, ACCUMULATOR, INSTRUCTION REGISTER, INDEX REGISTER

BASIC SINGLE ADDRESS ARCHITECTURE
- THE DATA BUS, FETCH AND EXECUTION CYCLES, REGISTER CYCLING AND DATA FLOW

MEMORY ADDRESSING MODES
- IMMEDIATE, DIRECT, RELATIVE AND INDEXED PAGING

A BASIC INSTRUCTION SET
- DATA MOVEMENT, ARITHMETICS, LOGICALS, PROGRAM CONTROL, STATUS AND FLAGS

A TYPICAL 4-BIT MICROPROCESSOR
- THE MCS-4 CHIP SET
- ROM AND RAM REQUIREMENTS
- A MINIMUM MCS-4 ARCHITECTURE
- SYSTEM TIMING AND CONTROL
- HARDWARE PROBLEMS AND SOLUTIONS
- EXPANSION OF MEMORY AND I/O

AN EASY TO USE 4-BIT PROTOTYPING SYSTEM
- STANDARD MEMORY INTERFACE
- UV ERASABLE ROMS
- TTL COMPATIBLE I/O PORTS
- CLOCK AND SYNC SYSTEM

INTRODUCTION TO PROGRAMMING
- USING THE REGISTERS, INSTRUCTION FORMAT, SINGLE AND DOUBLE WORD INSTRUCTIONS, A 4-BIT INSTRUCTION SET

WRITING A PROGRAM
FLOW CHARTING, PROGRAM CODING, USE OF SYMBOLIC AND MACHINE LANGUAGE

PROGRAMMING: DATA MOVEMENT
FUNCTION OF INDEX REGISTER, I/O PORT SELECTION, I/O EXECUTION, REGISTER-TO-REGISTER TRANSFERS, RAM DATA TRANSFERS

PROGRAMMING: BASIC ARITHMETIC OPERATIONS
HEXADECIMAL ADD AND SUBTRACT, TWO'S COMPLEMENT ARITHMETICS, SHIFT AND ROTATE COMMANDS

LABORATORY: USING THE "INTELLIGENT" ROM PROGRAMMER
ERASING THE EROM, ENTERING A PROGRAM, VERIFYING AND EDITING THE PROGRAM

PROGRAMMING: PROGRAM LOOPING AND DECISIONS
CONDITIONAL JUMPS, COMPARES, TESTING STATUS

PROGRAMMING: TIME DELAYS AND COUNTER
DEBOUNCE TECHNIQUES

LABORATORY: APPLICATIONS
GENERATING CONTROL SEQUENCES

PROGRAMMING: LOGICALS
AND, OR, NOT, XOR
BIT TESTING AND MANIPULATION

PROGRAMMING: USE OF SUBROUTINES
APPLICATION OF THE STACK, NESTING, SUBROUTINE EFFICIENCY

OTHER ROUTINES
MULTIPLY/DIVIDE, BCD OPERATIONS, KEYBOARD/DISPLAY, INTERRUPTS

LABORATORY: IMPLEMENTING PROGRAMMED LOGIC
PROGRAMMABLE SEQUENTIAL CONTROLLER

INTRODUCTION TO 8-BIT MICROPROCESSORS
A TYPICAL 8-BIT SYSTEM, THE MCS-8 SYSTEM ARCHITECTURE, TIMING AND CONTROL. CONFIGURING A MINIMUM SYSTEM, MEMORY AND I/O EXPANSION. HARDWARE AND INTERFACE REQUIREMENTS

AN EASY TO USE 8-BIT PROTOTYPING SYSTEM
EROM PROGRAM STORAGE, TTL COMPATIBLE I/O, CLOCK AND SYNC REQUIREMENTS

PROGRAMMING AN 8-BIT MACHINE
GENERAL PURPOSE REGISTERS, ADDRESS STACK, STATUS FLAGS, INTERRUPTS

AN EASY TO USE INSTRUCTION SET
REGISTER AND MEMORY INSTRUCTIONS, PROGRAM CONTROL, INPUT/OUTPUT, SUBROUTINES

LABORATORY: PROGRAMMED LOGIC APPLICATION
USING THE 8-BIT SYSTEM ANALYZER, DEBUGGING THE PROGRAM

LABORATORY: APPLICATION SEQUENTIAL ADAPTIVE CONTROLLER - TRAFFIC LIGHT

APPLICATIONS AND LIMITATIONS OF 8-BIT MICROPROCESSORS

ANALYSIS AND EVALUATION OF 8-BIT MICROPROCESSORS
INTEL MCS-8/8008, MCS-80/8080
ROCKWELL PPS-8
NATIONAL IMP-8
FAIRCHILD F8
MOSTEK 5065
MOTOROLA 6800
RCA COSMAC

LIST OF REFERENCES

INTERVIEWS

01. BRYER, BOB, SALES REPRESENTATIVE, HEWLETT-PACKARD, 2 CHOKE CHERRY ROAD, ROCKVILLE, MD 20850. (301) 948-6370.

02. DOAN, TERRY, CONSULTING ENGINEER, WTD INC., 2519 DEKALB PIKE, NORRISTOWN, PA 19401. (215) 277-2510.

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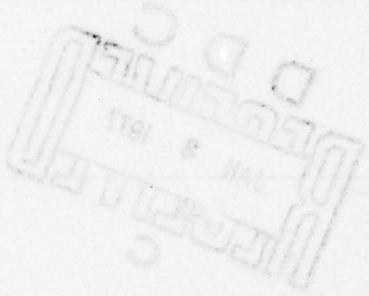

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